EUROPEAN PATENT APPLICATION

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(54) **Tracking filter and quadrature-phase reference generator.**

(57) A tracking filter has a tunable filter responsive to an input signal for producing a filtered output signal, a Hilbert transformer for producing an in-phase reference signal and a quadrature-phase reference signal from the filtered output signal, and a discriminator responsive to the input signal and the in-phase and quadrature-phase reference signals for producing a passband center frequency control signal and a passband width control signal for controlling the passband center frequency and the passband width of the tunable filter. The frequency discriminator performs complex demodulation of the input signal with the in-phase reference signals to produce respective in-phase and quadrature-phase baseband signals which are low-pass filtered. The quadrature-phase baseband signal is divided by the in-phase baseband signal. The quotient is integrated to produce the passband center frequency control signal. Preferably the baseband signals are also filtered by adjustable filters having passband center frequencies and passband widths controlled in response to the passband center frequency control signal and the passband width control signal, respectively. Preferably the tracking filter is a digital filter.

FIG. 15A
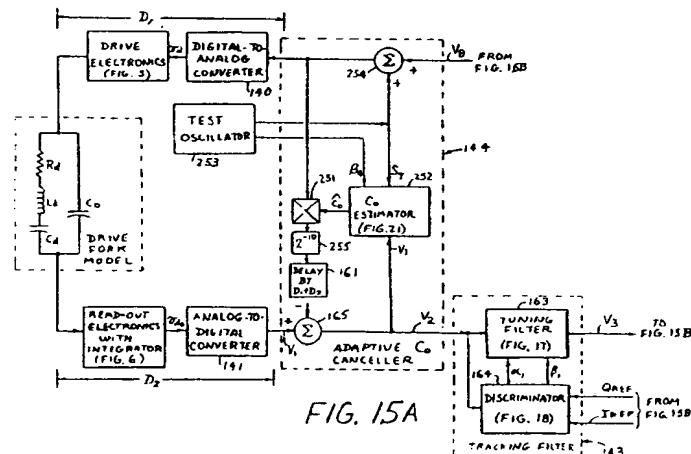
BACKGROUND OF THE INVENTION

1. Field of the Invention.

5   The present invention relates generally to digital signal processing, and more particularly to signal processing for a quartz angular-rate sensor or solid-state gyroscope.

2. Background Art.

10   Angular-rate sensors are essential components of navigational and inertial guidance systems of aircraft, spacecraft, ships, and missiles. Traditionally, mechanical gyroscopes were used for angular rate sensing. More recently, laser ring gyros and vibrating quartz gyros have been developed that have characteristics superior to mechanical gyroscopes.

A particularly economical vibrating quartz gyro is made by acid etching of a quartz wafer and has two 15 pairs of parallel tines in an "H" configuration. Such a quartz gyro is described, for example, in Fersht et al. U.S. Patent 5,056,366 and Staudte U.S. Patent Re 32,931. One pair of tines (the drive tines) is driven by an oscillator so that the tines move toward each other and away from each other. Rotational motion of the tines about the central longitudinal axis of the "H" causes the vibration of the drive tines to couple, by coriolis force, to the other pair of tines (the pick-off tines). The coriolis force causes the pick-up tines to vibrate in 20 such a way that when one pick-off tine moves in one traverse direction perpendicular to the plane of the "H", the other pick-off tine moves in the opposite transverse direction perpendicular to the plane of the "H". The force, which drives the pick-off tines, is proportional to the cross-product of the angular rate of rotation Ω (e.g., radians per second), and the linear velocity of the drive tines (e.g., meters per second). Metal film pads are plated onto the tines for piezoelectric coupling to these vibrations of the tines. In the electrical 25 pick-off signal, the angular rate of rotation of the quartz gyro about the longitudinal axis appears as double-sideband suppressed-carrier (DSSC) modulation of input angular rate; the carrier frequency is the frequency of oscillation of the drive tines. Therefore, an angular-rate signal can be recovered from the pick-off signal by a synchronous demodulator.

Analog circuits have been used for exciting the quartz gyro and for synchronous demodulation of the 30 pick-off signal. Analog circuits, however, are subject to voltage offsets and drift of component values due to temperature variations and aging. These problems are particularly troublesome due to peculiarities of the quartz gyro that are not apparent from the simplified or "first order" operating characteristics as described above. One problem is related to the resonant frequencies of the drive tines and the pick-off tines. It is undesirable for the pick-off tines to have the same resonant frequency as the drive tines because of the 35 extreme difficulty of removing the dynamics of the pick-off tines from the pick-off signal. If the pick-off tines did have the same resonant frequency as the drive tines, then a maximum amplitude response would be obtained from the pick-off tines, but the angular-rate signal would be a very non-linear function of the angular rate. The resonant frequency of the pick-off tines, however, must be tuned relatively closely to the resonant frequency of the drive tines, or else the dynamic range of the angular-rate signal is limited by 40 noise. Therefore, some resonant frequency offset is required between the drive tines and the pick-off tines. This compromise in resonant frequency offset is to an extent dependent on the bandwidth of the angular-rate signal. In particular, the pick-off tines have a two-pole resonance characteristic, giving a second-order response ($\approx 1/(\omega^2 - \omega_o^2)$) far away from the resonant frequency (ω_o). In practice, these considerations dictate that the difference between the resonant frequency of the drive tines and the resonant frequency of the 45 pick-off tines should be about twice the bandwidth of the angular rate to be sensed by the quartz gyro. A typical quartz gyro for inertial navigation applications, for example, has a drive resonant frequency of about 10 kilohertz, a Q of about 18,000, and a difference of about 100 Hz between the drive resonant frequency and the pick-off resonant frequency. The pick-up tines, for example, have the higher resonant frequency. This difference in resonant frequencies causes the amplitude of the angular-rate signal to be dependent on 50 the frequency as well as the amplitude of vibration of the drive tines. Moreover, the temperature dependence of the difference between the drive and pick-off resonant frequencies is the most critical temperature dependent parameter of the quartz gyro.

To obtain sufficient performance for inertial navigation, the analog circuits associated with the quartz gyro have been relatively complex and expensive. Moreover, it is estimated that the limitations of the prior-55 art analog circuitry causes the performance of the quartz gyro to be about an order of magnitude less than that theoretically possible and attainable by sufficiently complex digital signal processing.

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SUMMARY OF THE INVENTION

In accordance with a basic aspect of the present invention, there is provided a method of filtering an input signal. The method includes the steps of: passing the input signal through a filter having an adjustable
5 passband center frequency to produce an output signal; producing an in-phase reference signal and a quadrature-phase reference signal from the filtered signal; demodulating the input signal with the in-phase reference signal and the quadrature-phase reference signal to produce a frequency-control signal; and adjusting the passband center frequency of the adjustable filter in response to the frequency-control signal.

In accordance with another aspect, the invention provides a tracking filter. The tracking filter includes: a
10 tunable filter responsive to an input signal for producing a filtered signal on an output, the tunable filter having an adjustable passband center frequency responsive to a frequency control signal; a reference frequency generator having an input connected to the output for producing an in-phase reference signal and a quadrature-phase reference signal in response to the filtered signal; and a frequency discriminator responsive to the input signal and connected to the reference frequency generator and the tunable filter for
15 producing the frequency control signal by complex demodulation of the input signal with the in-phase reference signal and the quadrature-phase reference signal.

In accordance with a further aspect, the invention provides a tracking filter including a tunable filter, a Hilbert transformer, and a discriminator. The tunable filter is responsive to an input signal for producing a filtered signal on an output. The tunable filter has an adjustable passband center frequency responsive to a
20 frequency control signal. The tunable filter also has an adjustable passband width responsive to a passband-width control signal. The Hilbert transformer has an input connected to the output of the tuning filter for producing an in-phase reference signal and a quadrature-phase reference signal in response to the filtered signal. The frequency discriminator is responsive to the input signal and connected to the reference frequency generator and the tunable filter for producing the frequency control signal and the passband-
25 width control signal by complex demodulation of the input signal with the in-phase reference signal and the quadrature-phase reference signal.

In a preferred form of construction, the frequency discriminator includes a first multiplier for multiplying the in-phase reference signal by the input signal to produce an in-phase product signal, and a second multiplier for multiplying the quadrature-phase reference signal by the input signal to produce a quadrature-
30 phase product signal. The frequency discriminator also has a first lowpass filter connected to the first multiplier for filtering the in-phase product signal to produce a filtered in-phase product signal, a second lowpass filter connected to the second multiplier for filtering the quadrature-phase product signal to produce a filtered quadrature-phase product signal, and a divider connected to the first lowpass filter and the second lowpass filter for dividing the filtered quadrature-phase product signal by the filtered in-phase product signal
35 to produce a quotient signal. The frequency discriminator further has an integrator connected to the divider for integrating the quotient signal to produce the frequency control signal, and an absolute value generator connected to the divider for producing the bandwidth control signal from the absolute value of the quotient signal. For additional noise rejection, the frequency discriminator also includes a first adjustable notch filter connected between the first lowpass filter and the divider, and a second adjustable notch filter connected
40 between the second lowpass filter and the divider. Each of the first adjustable notch filter and the second adjustable notch filter has a frequency control input connected to the integrator for receiving the frequency control signal, and a passband-width control input connected to the absolute value generator for receiving the passband-width control signal.

45 ## BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the present invention will become apparent upon reading the following detailed description and upon reference to the drawings, in which:
FIG. 1 is a perspective view of an inertial measurement unit incorporating the present invention;
50 FIG. 2 is a pictorial view of a mounting arrangement for accelerometers and quartz angular-rate sensors used in the inertial measurement unit of FIG. 1;
FIG. 3 is a plan view of one of the quartz angular-rate sensors of FIG. 2;
FIG. 4 is a perspective view of a central portion of the quartz angular-rate sensor of FIG. 3;
FIG. 5 is a cross-section of drive tines of the quartz angular-rate sensor of FIG. 4 along section line 5-5
55 in FIG. 4;
FIG. 6 is a cross-section of the drive tines of the quartz angular-rate sensor of FIG. 4 along section line 6-6 if FIG. 4;

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FIG. 7 is a cross-section of pick-up tines of the quartz angular-rate sensor of FIG. 4 along section line 7-7 in FIG. 4;

FIG. 8 is a block diagram of a conventional system for exciting the quartz rate sensor of FIG. 4 and synchronously detecting an angular-rate signal;

5 FIG. 9 is a perspective view showing an alternative construction for electrodes on drive tines of a quartz angular-rate sensor;

FIG. 10 is a cross-section of the drive tines of the quartz angular-rate sensor of FIG. 9 along section line 10-10 of FIG. 9;

FIG. 11 is a schematic diagram of analog computational circuits for computing drive signals for the drive
10 electrodes as shown in FIG. 10;

FIG. 12 is a conventional circuit for exciting the quartz rate sensor of FIG. 9 and synchronously detecting an angular-rate signal;

FIG. 13 is a block diagram of an analog drive circuit used in FIG. 12 for exciting the quartz rate sensor;

FIG. 14 is a block diagram of a quartz rate sensor system using digital signal processing in accordance
15 with the present invention;

FIGs. 15A and 15B together comprise a more detailed block diagram of the driver circuits for the quartz rate sensor system of FIG. 14;

FIG. 16 is a block diagram of a delay unit for providing a delay that is not an integral number of sampling periods;

20 FIG. 17 is a schematic diagram of a tuning filter introduced in FIG. 15A;

FIG. 18 is a schematic diagram of a discriminator introduced in FIG. 15A;

FIG. 19 is a schematic diagram of a Hilbert transformer introduced in FIG. 15B;

FIG. 20 is a schematic diagram of a rotator introduced in FIG. 15B; and

FIG. 21 is a schematic diagram of a shunt capacitance estimator introduced in FIG. 15A;
25 FIG. 22 is a schematic diagram of a lead/lag network introduced in FIG. 19;

FIG. 23 is a schematic diagram of an automatic gain control introduced in FIG. 15B;

FIG. 24 is a schematic diagram of a test oscillator introduced in FIG. 15A; and

FIG. 25 is a flowchart of a method for selectively resetting the test oscillator of FIG. 24 to prevent amplitude drift due to accumulation of round-off error.

30 While the invention will be described in connection with certain preferred embodiments, it is not intended that the invention should be limited to these particular embodiments. On the contrary, the invention is intended to include all modifications, alternatives, and equivalent arrangements as may be included within the scope of the appended claims.

35 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Turning now to the drawings, there is shown in FIG. 1 a schematic perspective view of an inertial measurement unit generally designated 50 incorporating the present invention. The inertial measurement unit includes a block of sensors 51, electronic circuit boards 52, and an electrical connector 53. The inertial
40 measurement unit 50 provides an angular velocity signal and a linear acceleration signal with respect to each of three orthogonal directions. The angular velocity and linear acceleration signals have a 50 Hz bandwidth.

Turning now to FIG. 2, there is shown a pictorial view of the sensor block 51. The block is made of a rigid material such as aluminum or polycarbonate. A quartz angular-rate sensor or a vibrating quartz
45 accelerometer is mounted into each of the six faces of the block 51. The sensors include quartz angular-rate sensors 61, 62, and 63 mounted on the faces facing the +x, +y, and +z directions. The sensors include vibrating quartz accelerometers 64, 65, and 66 mounted on the faces facing the -x, -y, and -z directions, respectively.

The present invention concerns signal processing for the quartz angular-rate sensors 61, 62, and 63.
50 The quartz angular-rate sensors operate entirely independent of the vibrating quartz accelerometers. Therefore, the vibrating quartz accelerometers 64, 65, 66 are not pertinent to the present invention and will not be described in any further detail.

Turning now to FIG. 3, there is shown a more detailed view of the quartz angular-rate sensor 62. The sensor 62 is fabricated from a z-cut quartz wafer using conventional photolithographic and acid etch batch
55 processes, and can be purchased from Systron Donner Corporation of Concord, California. The sensor has a frame 71 attached to an "H"-shaped section by a pair of bridges 73, 74. The "H"-shaped section 72 has a pair of drive tines 75, 76, and a pair of pick-up tines 77, 78.

Turning now to FIG. 4, there is shown a number of metal film electrodes deposited on the tines 75, 76, 77, and 78. The drive tines 75, 76 are provided with drive electrodes 81, 82, 83, 84, 85, 86, 87, 88, as further shown in FIG. 5. The drive electrodes are driven by a complementary drive signal V_d, as shown in FIG. 5, to excite a mode of vibration in the drive tines 75, 76 in which the drive tines first move toward each

5 other in the x direction, as shown in FIG. 4, and then away from each other, during each cycle of vibration. To sustain such a mode of vibration, the complementary drive signal V_d must be tuned to the resonant frequency of the drive tines. As shown in FIG. 5, a unity-gain inverting amplifier 80 is used in providing the complementary drive signal from a single-ended drive signal.

To drive the drive tines 75, 76 at their resonant frequency, the drive tines are excited in response to

10 sensing their elastic deformation. For this purpose, a second set of metal film electrodes 89 to 96, as further shown in FIG. 6, are disposed on the drive tines 75, 76 at locations of maximum elastic deformation where the tines are joined to the central portion of the H-shaped structure 72, as shown in FIG. 4. These electrodes 89 to 96 are connected to a conventional amplifier 110 providing a signal v_{do} indicating the elastic deformation of the drive tines 75, 76.

15 As shown in FIG. 4, the vibration of the pick-up tines 77, 78 is sensed by metal film electrodes 101 to 108 deposited on the pick-up tines. As further shown in FIG. 7, the pick-up electrodes 101 to 108 are connected to a conventional amplifier 111 to provide a signal v, indicating the vibration of the pick-up tines.

Turning now to FIG. 8, there is shown a conventional circuit for obtaining an angular-rate signal Ω from the crystal rate sensor and amplifiers as shown in FIGs. 5, 6, and 7. A driver circuit 115 is responsive to the

20 signal v_{do} to produce a drive signal v_d at the resonant frequency of oscillation of the drive tines (75, 76 in FIG. 4). Moreover, the driver circuit 115 insures that the amplitude of vibration of the drive tines 75, 76 is substantially constant. Further, the driver 115 supplies a signal at the frequency of oscillation f_o to a synchronous detector 116, such as a balanced modulator, that modulates the pick-up signal v, to detect the angular-rate information. A low-pass filter 117 extracts the angular-rate signal Ω from the output of the

25 synchronous detector 116.

Turning now to FIG. 9, there is shown an alternative construction in which pairs of drive electrodes 81a, 81b, to 88a, 88b, are deposited on the drive tines 75', 76', as further shown in FIG. 10. In this alternative construction, the drive electrodes 81a, 81b, to 88a, 88b are excited with a nulling signal v_n in addition to the drive signal v_d. The nulling signal v_n excites vibrations of the drive tines 75', 76' that directly couple to the

30 pick-up tines (not shown), and therefore the nulling signal can be adjusted to minimize or null the vibration of the pick-up tines 77, 78.

As shown in FIG. 11, analog computational circuits 120 receive a single-ended drive signal V_d and a single-ended null signal v_n to produce electrical signals ($-v_d + v_n$, $-v_d - v_n$, $v_d - v_n$, $-v_d - v_n$) that are applied to the pairs of drive electrodes (81a, 81b, to 88a, 88b in FIG. 10). These analog computational circuits 120 include

35 an operational amplifier 120 wired as a differential amplifier, an operational amplifier 121 wired as an inverting summing amplifier, an operational amplifier 122 wired as an inverting unity gain amplifier, and an operational amplifier 123 wired as an inverting unity gain amplifier.

When the quartz rate sensor is operated such that a null signal v_n nulls out the pick-up signal v_r, the crystal rate sensor is said to be operated in a "closed loop" mode. A circuit for operating the quartz rate

40 sensor in such a "closed-loop" mode is shown in FIG. 12. The circuit includes a driver 115', a synchronous detector 116', and a low-pass filter 117' that are similar to the driver 115, synchronous detector 116, and low-pass filter 117 introduced in FIG. 8. However, the circuit in FIG. 12 further includes a baseband servo equalizer and feedback amplifier 118, a balanced modulator 119 for supplying the null signal v_n at the frequency of oscillation f_o but having an amplitude controlled by negative feedback to null out the pick-up

45 signal v_r, and the analog computational circuits 120 shown in FIG. 11. Therefore, the amplifier 118 provides the angular-rate signal Ω.

Turning now to FIG. 13, there is shown a block diagram for the driver circuit 115 of FIG. 8. The driver circuit 115 includes a bandpass filter 124 that filters the v_{do} signal and is tuned for a maximum response at the resonant frequency f_o of the drive tines. The output of the bandpass filter 124 is fed through a phase-

50 adjusting circuit 125 that is adjusted for (360)(n) degree (n is any integer) phase shift around the entire drive loop, through the drive electrodes (81 to 88 in FIGS. 4 and 5), through the physics of the drive fork, through the drive sensing electrodes (89 to 96 in FIGS. 4. and 6), and through the electronics in FIG. 13. The output of the phase-adjusting circuit is fed to an automatic gain control 126 that senses the amplitude of the signal from the phase-adjusting circuit and generates a gain control voltage responsive to the difference between

55 the amplitude of the signal from the phase-adjusting circuit 125 and an amplitude setting. The amplitude setting may be adjusted, for example, in response to calibrating the angular-rate sensor by subjecting the sensor to a precise rate of angular rotation and adjusting the amplitude setting so that the angular-rate signal Ω precisely indicates the rate of angular rotation. The gain-control voltage from the automatic gain

control adjusts the gain of a linear amplifier 127 that amplifies the output of the phase-adjusting circuit 125 to produce the drive signal v_d. The linear amplifier, for example, is an operational transconductance amplifier, such as RCA part No. CA3080.

Turning now to FIG. 14, there is shown a block diagram of a quartz rate sensor system using digital signal processing in accordance with the present invention. The drive signal v_d to the quartz rate sensor is produced by a digital-to-analog converter 140 in response to a digital value v_9. The digital-to-analog converter 140, for example, is a 16-bit monolithic voltage output D/A converter such as Analog Devices part no. AD569, or an Analog Devices 18-bit digital-to-analog converter part no. AD1139. The output voltage v_{do} indicating the level of excitation of the quartz rate sensor is sampled by an analog-to-digital converter 141 to produce a digital signal v_1. In a similar fashion, the pick-off signal v_r is sampled by an analog-to-digital converter 142 to produce a digital signal v_{10}. The analog-to-digital converter 141 and the analog-to-digital converter 142, for example, are 16-bit 100k SPS sampling analog-to-digital converters, such as the Analog Devices part no. AD676, which uses a switched-capacitor/charge redistribution architecture. The digital-to-analog converter 140, the analog-to-digital converter 141, and the analog-to-digital converter 142 are all clocked in synchronism at a fixed sampling rate, which is, for example, 42 kHz. For the inertial measurement unit as shown in FIG. 1, the circuit as shown in FIG. 14 is replicated three times, and all of the digital-to-analog converters and analog-to-digital converters are clocked in synchronism by a common system clock (not shown) which is external to the inertial measurement unit 50. The system clock, for example, is part of an avionics package that receives the angular rate and linear acceleration information from the inertial measurement unit 50.

Aside from the quartz rate sensor and amplifiers, and the digital-to-analog converter 140 and the analog-to-digital converters 141, 142 in FIG. 14, all of the other components are synchronous digital logic circuits which could be implemented as either a programmed data processor or as hard-wired logic, for example, in an application-specific integrated circuit. The synchronous digital circuits, for example, could be implemented in a Star Semiconductor SPROC programmable digital signal processing (DSP) integrated circuit which is designed for fixed-point 24-bit arithmetic.

In order to excite the quartz rate sensor at the resonant frequency of the drive tines (75 and 76 in FIG. 4), the digital circuitry in FIG. 14 includes an adaptive C_o canceler 144 for canceling undesired effects of shunt capacitance C_o of the drive tines, a tracking filter 143 that tracks the resonant frequency of the drive tines, a reference signal generator and loop phase shifter 145, and an automatic gain control 146.

The adaptive C_o canceler 144 adds a correction signal to the output v_1 of the analog-to-digital converter 141 in order to cancel a similar signal passing from the drive signal v_d and through the shunt capacitance C_o of the drive tines and appearing in the input signal v_{do}.

The signal v_{do} includes a noise-contaminated demodulation reference signal that is slowly drifting in frequency. The tracking filter 143 automatically adjusts its passband width and passband center frequency in order to extract the demodulation reference signal. As will be further described below with reference to FIG. 15A, the tracking filter 143 is part of a tracking loop that tracks the frequency of the demodulation reference signal and that reduces the passband width of the tracking filter when the demodulation reference signal is detected. Therefore, the output v_3 of the tracking filter 143 is a very clean sinusoid.

The reference signal generator and loop phase shifter 145 provides two reference signals I'_{REF} and Q'_{REF} which are exactly 90° apart in phase, in order to demodulate the angular rate signal Ω from the pick-off signal v_r. The reference signal generator and loop phase shifter 145 also provides exactly an integral number $\underline{n}$ times 360° of phase shift around the drive loop. Therefore the drive tines of the quartz rate sensor are driven at their resonant frequency, which occurs when there is zero phase shift through the drive tines.

The automatic gain control 146 provides exactly unity gain around the drive loop by exciting the drive tines so that the reference frequency signal extracted by the tracking filter 143 has a constant amplitude.

In order to demodulate the angular rate signal Ω from the pick-off signal v_r, a first multiplier 147 multiplies the signal v_{10} from the analog-to-digital converter 142 by the in-phase reference signal I'_{REF} to produce an in-phase product value (i), and a second multiplier 148 multiplies the signal v_{10} by the quadrature-phase signal Q'_{REF} to produce a quadrature-phase product value (q). The in-phase value (i) is received in an I-channel filter 149, which is a conventional decimating digital low-pass filter, to provide a filtered value I at a lower rate such as 600 Hz. In a similar fashion, the quadrature-phase value (q) is received in a Q-channel filter 150, which also is a conventional digital low-pass decimating filter, to provide a filtered value Q at a lower rate such as 600 Hz.

Because the circuit of FIG. 14 provides both in-phase and quadrature-phase detected signals, any phase shift or tuning error between the reference signal I_{REF} at the frequency f_o and the suppressed carrier in the pick-off signal v_r can be corrected by a rotation of the complex vector $I + iQ$, and this rotation is

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performed by a numerical phase adjustment in the reference signal generator 145, as will be described below with reference to FIG. 20. For example, all of the detected angular-rate signal should appear in the in-phase channel I of FIG. 14. In practice, however, there will be some phase offset causing some of the angular-rate signal to appear in the quadrature-phase channel Q.

5 In general, the angular-rate signal Ω should have a sign that is the sign of the signal in the in-phase channel I and a corrected magnitude equal to the square root of $I^2 + Q^2$. In fact, imperfections within the instrument, alignment errors, and capacitive coupling cause extraneous contributions to the I and Q signals which should be eliminated by calibration and post-processing by computing Ω from the signals I and Q after removal of the extraneous contributions. Compensation 151 for the extraneous contributions could be
10 performed by referencing calibration data retrieved from calibration tables programmed in non-volatile memory.

Turning now to FIGs. 15A and 15B, there is shown a more detailed block diagram of the drive loop. As shown in FIG. 15A, the drive fork is electrically modeled by the shunt capacitance C_o representing primarily inter-electrode capacitance, and a series resistance R_d, a series inductance L_d, and a series capacitance C_d.
15 The resonant frequency of the drive fork is determined primarily by the product of the series inductance L_d and the series capacitance C_d.

As further shown in FIG. 15A, the drive electronics of FIG. 5 and the digital-to-analog converter 140 are modeled as a time delay D_1. In a similar fashion, the read-out electronics with its integrator of FIG. 6, and the analog-to-digital converter 141, are modeled as having a combined delay of D_2. The sum of D_1 and D_2
20 represents a delay $D_1 + D_2$ that is measured for a signal at the nominal drive resonant frequency and is then assumed to be constant. This constant value of $D_1 + D_2$ is divided by the sampling periods $T = 1/f_s$, where f_s is the sampling frequency of the analog-to-digital converter 141, to express the total delay $D_1 + D_2$ as an the sum of an integer i and a fraction δ in units of T. The integer i determines the maximum number of storage registers that are used in each of a delay block 161 in the adaptive C_o canceler, and in a delay
25 block 162 in the reference signal generator and loop phase shifter 145 as shown in FIG. 15B.

Turning for a moment to FIG. 16, there is shown a schematic diagram of a circuit for the delay block 161, which is identical to the delay block 162. The delay block 161 includes a delay unit 154 for delaying the input signal S_{IN} by i periods of T. The delay unit 161 is conventional, and includes, for example, i registers clocked in synchronism at the sampling frequency f_s and connected in a shift-register arrange-
30 ment. The delay unit 161 further includes a delay unit 155 that provides an additional delay of one sample period T. The delay unit 155, for example, includes a single register. To provide an output signal S_{OUT} approximating the input signal S_{IN} delayed by $(i + \delta)T$, the output signal S_{OUT} is computed by interpolation between the output of the delay unit 154 and the output of the delay unit 155. As shown in FIG. 16, for example, a scaling unit or multiplier 159 scales the difference between the output of the delay unit 154 and
35 a delay unit 156 by a factor of A. A summer or adder 157 adds the output of the delay unit 155 to the output of the scaling unit 159 to produce an intermediate signal S_{int}. The intermediate signal S_{int} is delayed for one sampling period T in the delay unit 156. A subtractor 158 subtracts the output of the delay unit 154 from the output of the delay unit 156 to produce the input to the scaling unit 159. A subtractor 158A subtracts the intermediate signal S_{int} from the output of delay element 156A. An adder 157A combines the
40 output of delay unit 156 and the output of the scaling unit 159A to generate the signal S_{OUT}. The input to delay element 156A is S_{OUT}; the input to multiplier 159A is the output of subtractor 158A. The components 155 to 159 and 156A to 159A in FIG. 16 therefore comprise an all-pass filter that provides a phase shift that approximates the required fractional delay of δT.

Returning now to FIG. 15A, the tracking filter 143 includes a tuning filter 163 and a discriminator 164.
45 The passband width of the tuning filter 163 is controlled by a parameter α_1, and the passband-center frequency of the tuning filter is controlled by a parameter β_1. The analog-to-digital converter output v_1 passes through an adder 165 in the adaptive C_o canceler 144 to become a signal v_2 which is in turn the input to the tuning filter 163. The tuning filter output is signal v_3.

The signal v_3 drives a Hilbert transformer 167, which is a kind of non-recursive digital filter that is a very
50 precise 90° phase-shifting network. An example of the Hilbert transformer is further described below with reference to FIG. 19. The Hilbert transformer provides an in-phase reference I_{REF}, which is a delayed copy of the input signal v_3, and a quadrature-phase output Q_{REF} that lags the in-phase reference I_{REF} by 90°. These two reference signals I_{REF} and Q_{REF} are fed back to the discriminator 164 in the tracking filter 143 of FIG. 15A.

55 Turning for a moment now to FIG. 17, the tracking filter 163 is shown in greater detail. It should be noted that the symbols in FIG. 17 are conventional symbols for representing a digital filter. An adder or subtractor unit is designated by a circle including the Greek letter Σ and the input nodes being labeled plus or minus. The tracking filter in FIG. 17, for example, includes six such summing nodes 168, 169, 170, 171,

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172, and 173. A multiplier is designated by a box circumscribing an X, such as the multipliers 175 and 176 in FIG. 17, which multiply by α_1 and β_1, respectively. A delay by a fixed integral number n of sampling periods T is denoted by a box including the z transform symbol z^{-n}. The blocks 177 and 178, for example, each provide a delay of one sampling period T, which is produced, for example, by a register storage and recall operation in a programmed digital signal processor. A scaling by a fixed constant is represented by a box including the constant. The tracking filter 163, for example, includes a box 179 representing a scaling of one-half, which is conveniently obtained by an arithmetic right shift operation in a programmed digital signal processor.

Turning now to FIG. 18, there is shown a schematic diagram of the discriminator 164. The input signal v_2 is delayed in a delay unit 191 such as a shift register having a delay that is the delay to the center tap of the Hilbert transformer 167 of FIG. 15B. For example, the Hilbert transformer 167 provides a delay of nine sampling periods T. Therefore, in this example, the delay unit 191 should provide a delay of nine sampling periods T.

In any case, the phase shift between the output signal v_{12} of the delay unit 191 and the reference signal I_{REF} is zero when the passband center-frequency of the tuning filter (163 in FIG. 17) is tuned to frequency of the signal v_{12}. When the passband center-frequency of the tuning filter is not tuned to frequency of the signal v_{12}, then there will be a phase shift between the signal v_{12} and the reference signal I_{REF}, and this phase shift will be an indication of the tuning error of the tuning filter. Therefore, the discriminator 164 in FIG. 18 can detect any phase shift between the signal v_{12} and the reference signal I_{REF}, and adjust the bandpass center-frequency control signal β_1 in response to the detected phase shift, in order to reduce the phase shift and the tuning error to zero.

Within the discriminator 164, the delayed signal v_{12} is complex-demodulated by the reference signals I_{REF} and Q_{REF} by a pair of multipliers 192, 193, low-pass filtered by low-pass filters 194, 195, and notch-filtered by adjustable notch filters 196, 197 to remove the double-frequency components generated by the multipliers 192, 193. The signal N from the adjustable notch filter 197 is a measure of the tuning error of the tuning filter 163 of FIG. 15A, although its amplitude is also a function of the amplitude of the input signal v_2. Therefore, a substantially amplitude-independent tuning error signal is produced by a divider 198 that divides the signal N from the notch filter 197 from the output D of the notch filter 196. Moreover, to prevent an inaccurate result when the output D is approximately zero, the quotient in this case should be forced to zero.

The tuning error signal v_{13} from the divider 198 is a direct candidate for determining the desired passband-width of the tuning filter 163 in FIG. 15A. In particular, the tuning parameter α_1 is determined by an absolute value unit 199 which produces the absolute value of the tuning error signal v_{13}, a subtractor 200 which subtracts the absolute value from a predetermined constant $\alpha_{1\,max}$, and a limiter 201 which limits the difference to within reasonable limits, in order to produce α_1. The constant $\alpha_{1\,max}$, for example, has a value of 0.999, and α_1 is limited so that $0.4 \leq \alpha_1 \leq 0.999$. In effect, the passband-width control parameter α_1 is determined so that the tuning filter 163 is adjusted to have a passband width of at least twice the difference between the frequency of the signal v_1 and the frequency of the reference signals I_{REF} and Q_{REF}.

The passband frequency parameter β_1 of the tuning filter 163 is generated by an integrator or accumulator 202 which integrates the tuning error signal v_{13} from the divider 198. (The integrator 202 is similar in construction to the accumulator 338 shown in FIG. 23, and the value of β_1 is limited to ± 1.) A tuning frequency parameter β' for the notch filters 196, 197 is generated from β_1 by a multiplier 203 which computes the square of β_1, a scaling unit 204 which scales the square by a factor of two, for example, by a left shift of one binary place, and by a subtractor 205 which subtracts a constant value of one from the output of the scaling unit 204. Each of the adjustable notch filters 196, 197 is similar to the tuning filter 163 as shown in FIG. 17, except that β' would be used instead of β_1, and all of the inputs to the adder 173 would carry plus signs.

Further details regarding the tracking filter 143 are disclosed in the tracking filter design program listed in Appendix I.

Turning now to FIG. 19, there is shown a schematic diagram of the Hilbert transformer 167. The input signal v_3 is successively delayed by either two sample periods T or one sample period T by delay units 211-220. The delay units 211-214 and 217-220 each provide a delay of two sampling periods T, and the delay units 215, 216 provide a delay of one sampling period T. The in-phase reference I_{REF} is produced by the output of the delay unit 215. The quadrature-phase reference Q_{REF} is a weighted sum of the input signal v_3 and the outputs of the delay units. In particular, a first row of subtractors 221 subtracts a respective one of the input signal v_3 or the outputs of one of the delay units 211-214 from the output of a respective one of the delay units 216-220. The differences are scaled by respective coefficients a_0-a_4 in a row of scaling units 222. The outputs of the scaling units 222 are summed together by a row of adders 223 to produce the

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quadrature-phase reference signal Q_{REF}.

As derived in Appendix II, an appropriate set of coefficients for the Hilbert transformer 167 are as follows:

$$a_0 = 0.6142410357$$
$$a_1 = 0.1529612327$$
$$a_2 = 0.0496214228$$
$$a_3 = 0.0127215311$$
$$a_4 = 0.0018368168$$

It should be noted that the Hilbert transformer 167 could be modified to increase or decrease the precision of the quadrature-phase reference Q_{REF} with a corresponding increase or decrease in computational complexity. For example, the delay units 211, 212, 219, and 220, their associated subtractors 224, 225, their associated multipliers 226, 227, and their associated adders 228 and 229 could be eliminated, in which case the input signal v_3 would feed directly to the delay unit 213. In this case, the Hilbert transformer would use only three multipliers, and the coefficients a_0, a_1, and a_2 would be changed to:

$$a_0' = 0.5868816329$$
$$a_1' = 0.099083914$$
$$a_2' = 0.0122024482$$

The in-phase reference I_{REF} and the quadrature-phase reference Q_{REF} from the Hilbert transformer 167 of FIG. 19 could be used directly for demodulating the pick-off signal v, from the quartz rate sensor. Preferably, however, a reference phase adjustment is provided by a rotator 241 in FIG. 15B that performs a complex rotation of the reference signals I_{REF} and Q_{REF} through a predetermined compensation angle α to produce a transformed in-phase reference signal I'_{REF} and Q'_{REF}.

Turning for a moment to FIG. 20, there is shown a schematic diagram of the rotator 241. The complex rotation is provided by four scaling units 242, 243, 244, and 245, a subtractor 246 which produces the transformed in-phase reference signal I'_{REF}, and an adder 247 which produces the transformed quadrature-phase reference signal Q'_{REF}. The compensation angle a is adjusted during calibration of the system, as described above with reference to FIG. 14, and the sine and cosine of the compensation angle are stored in nonvolatile memory. During the operation of the system, the sign and cosine of the compensation angle α are retrieved from non-volatile memory to be multiplied by the in-phase reference I_{REF} and the quadrature-phase reference Q_{REF} to perform the scaling functions of the scaling units 242, 243, 244, and 245.

Returning now to FIG. 15A, the signal v_1 from the analog-to-digital converter 141 is received by the subtractor 165 which subtracts a compensation signal to cancel a signal component from the shunt capacitance C_0 of the drive fork. This compensation signal is produced by a multiplier 251 which multiplies a capacitance estimate $\hat{C}_0$ by the signal v_3 which is a digital version of the drive signal v_d, and a scaler unit 255 which scales the product of the multiplier 251 by a factor of 2^{-10}, for example, by an arithmetic right shift by ten binary places. In this fashion, the C_0 canceler 144 is placed across the digital input and digital output lines between the input of the digital-to-analog converter 140 and the output of the analog-to-digital converter 141. The shunt path from the signal v_3 to v_2 cancels the shunt capacitive path through the drive fork.

The estimate of the capacitance $\hat{C}_0$ is generated by a C_0 estimator 252 responsive to a signal S_T from a test oscillator 253. Preferably the signal S_T from the test oscillator 253 is generated and used continuously for estimating the value of the shunt capacitance C_0. A single test oscillator 253 is used for providing the test signal S_T to the three quartz rate sensors in the inertial measurement unit 50 of FIG. 1. A suitable test oscillator will be described below with reference to FIG. 24.

The test oscillator 253 may also supply a tuning parameter β_4 indicating the frequency of the test signal S_T with reference to the sampling frequency f_s. If the tuning parameter β_4 were not provided by the test oscillator, then it could be generated by a circuit similar to the portion of FIG. 23 including the components 329 to 341 in FIG. 23. Alternatively, the test frequency S_T could be a predetermined fraction of the sampling frequency f_s, so that the tuning parameter β_4 could be a predetermined constant, and therefore need not be supplied by the test oscillator 253.

Since the admittance of the shunt capacitance C_0 increases with frequency, it is desirable for the test oscillator 253 to run at the highest practical frequency which is just under one-half of the sampling frequency f_s. At that frequency, the net shunt capacitance is $\Delta C_0 = C_0 - \hat{C}_0$. When the magnitude of the admittance of the net shunt capacitance ΔC_0 is approximately equal to the magnitude of the admittance of the series combination of the series resistance R_d, the inductance L_d, and the series capacitance C_d in the drive fork model, the equivalent circuit creates a complex-zero pair at the frequency of the test oscillator and the loop stops adjusting. For a 42 kHz sampling frequency, the test frequency would be limited to less than 21 kHz.

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In any event, the frequency of the test signal is selected to be different from the resonant frequency f_o of the drive fork, so that the amplitude of the returned signal component of the test signal appearing in the output signal v_{do} is proportional to the shunt capacitance C_o. The subtractor 165 determines the difference between the returned signal component of the test signal and a cancellation signal passing through the delay unit 161. The C_o estimator 252 is responsive to this residual signal at the test frequency. Therefore, the C_o estimator can determine the estimate $\widehat{C}_o$ that will minimize the residual at the test frequency in the signal v_3.

Turning now to FIG. 21, there is shown a schematic diagram of the C_o estimator 252. A multiplier 261 multiplies the signal v_2 by the test signal S_T to detect the residual of the test signal appearing in the signal v_2. The double frequency term in the product is filtered out by a notch filter including delay units 262 and 263, a multiplier 264 which multiplies the output of the first delay unit 262 by the tuning parameter β_4, and an adder 265 which adds the product from the multiplier 261 to the output of the second delay unit 263 and subtracts the product from the multiplier 264. The sum from the adder 265 passes through a lead/lag network 266 which is used for ensuring stability. The lead/lag network will be further described below with reference to FIG. 22. A multiplier 267 scales the output of the lead/lag network by a factor μ_1 that adjusts the loop gain for the estimation of the capacitance C_o. The factor μ_1, for example, is 2^{-10}. The product from the multiplier 267 is averaged in an accumulator including an adder 268, a unit amplitude limiter 269 having an output limited to ± 1, and a delay unit or accumulator register 270. The accumulator register 270 provides the scaled capacitance estimate $\widehat{C}_o$.

Turning now to FIG. 22, there is shown a schematic diagram of the lead/lag network 266 introduced in FIG. 21. The lead/lag network includes a first delay unit 281 which delays the input signal v_{IN} by one sampling period T, and a second delay unit 282 having a delay of one sampling period T and having a feedback path in order to provide the pole in the frequency response of the lead/lag network. A summer 283 sums the output of the second delay unit 282 with the input signal v_{IN}, and the sum is scaled by a scale factor having a value of

$$e^{-L\omega_o T}$$

in a scaling unit 284. The parameter L, for example, has a value of 5.9. A subtractor 285 subtracts the output of the first delay unit 281 from the output of the scaler 284 to provide a difference that is received by the second delay unit 282.

In order to produce the output signal v_{OUT} of the lead/lag network 266, a subtractor 286 subtracts the output from the subtractor 285 from the input v_{IN}, and a scaling unit 287 scales the difference by the factor of 1/2L. An adder 288 adds the output of the subtractor 285 to the input signal v_{IN}, and a scaling unit 289 scales the sum by the factor L/2. Finally, an adder 290 adds the output of the scaling unit 287 to the output of the scaling unit 289 to produce the output signal v_{OUT}.

Turning now to FIG. 15B, there are shown further details of the reference signal generator and loop phase shifter 145. To provide exactly an integer number $\underline{n}$ times 360° of phase shift around loop and zero degrees of phase shift across the drive tines, the reference signal generator and loop phase shifter 145 shifts the signal v_3 by an adjustable phase angle to produce the signal v_7. The phase shift can be continuously adjusted by up to plus and minus 90° in response to a signal from a phase-error accumulator generally designated 300. The phase-error accumulator 300 has an adder 301, a limiter 302, and a delay unit or accumulator register 303. The limiter 302 limits the value in the delay unit 303 to within plus one and minus one corresponding to the arcsine of the adjustable angle of phase shift. The cosine corresponding to this angle of phase adjustment is computed by a multiplier 304 and a functional unit 305 which computes the square root of one minus x, where x is the square of the sine value. Preferably, the square root of one minus x is computed by an 8-term Chebychev polynomial approximation:

$$\sqrt{1-x} \approx \sum_{i=0}^{7} a_i x^i$$

where:

a_0 = 1
a_1 = -0.800044 hexadecimal
a_2 = -0.1FF585 hexadecimal

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a_3 = -0.109BC8 hexadecimal
a_4 = -0.05A0C5 hexadecimal
a_5 = -0.178DE2 hexadecimal
a_6 = 0.1B649B hexadecimal
a_7 = -0.2093C3 hexadecimal

A first multiplier 306 multiplies the in-phase channel reference I_{REF} by the cosine value from the functional unit 305 to produce a first product, and a second multiplier 307 multiplies the quadrature-phase reference Q_{REF} by the sine value from the delay unit 303 to produce a second product. In a subtractor 308, the first product from the first multiplier 306 is subtracted from the second product from the second multiplier 307 to produce a signal v_4. An additional phase shift equal to the integer K times 360° f_o/f_s is provided by the delay unit 166. For a sampling frequency of 42 kHz and a nominal drive fork resonant frequency of 10 kHz, the delay unit 166 therefore provides a coarse phase adjustment by phase steps of somewhat less than 90°. This coarse adjustment, however, is all that is necessary so that the phase error can be eliminated by the continuous adjustment made in response to the phase error signal in the phase-error accumulator 300.

The phase-error accumulator 300 is responsive to a phase comparison between the phase of the signal v_3 and the phase of the signal v_7 after a delay through the delay unit 162. At resonance, there is no phase shift through the drive fork, so that any phase shift that does appear on the signal passing through the drive fork is a measure of the frequency error; i.e., how far the frequency of oscillation is from the resonant frequency of the fork. As illustrated in FIG. 15, there is a phase shift of 90° due to the integrator in the read-out electronics of FIG. 6, and there is a time delay of D_1 and D_2 from the signal v_9 to the signal v_1 even when there is a zero phase shift through the drive fork. Therefore, by delaying the signal v_7 through the delay unit 162, and comparing the phase of the output of the delay unit 162 with the signal v_3 to obtain a 90° phase difference, then the phase across the drive fork can be set to zero, as desired.

A multiplier 309 multiplies the signal v_3 by the output of the delay unit 162 to provide a phase-error signal that is zero as desired for a 90° phase difference, and the phase-error accumulator 300 is responsive to this phase error signal so that the servo-action of the phase-error adjustment directs the signal from the delay unit 162 to lead the signal v_3 by 90°, thereby pulling the frequency error towards zero. The output of the multiplier 309 is a zero-frequency signal proportional to the phase error, plus a double frequency term that is removed by a notch filter 310. The notch filter 310 includes a first delay unit 311, a second delay unit 312, a multiplier 313, and an adder 314. A lead/lag network 315, similar to the lead/lag network 266 shown in FIG. 22, and a gain scaler 316 provide stable close-loop servo characteristics.

Turning now to FIG. 23, there is shown a schematic diagram of the automatic gain control 146 shown in FIG. 14 and in FIG. 15B. The automatic gain control has a multiplier 321 at the top of the figure that multiplies the signal v_7 by a variable gain factor to produce the signal v_8. This gain factor is the output of an accumulator generally designated 322, which includes an adder 323, a limiter 324, and a delay unit or accumulator register 325. The accumulator 322 functions as an integrator and lowpass filter. The accumulator 322 is responsive to the error in the comparison of the amplitude of the signal v_3 and a reference level set by a reference signal v_{REF}. In particular, a multiplier 326 computes the square of the signal v_3, and the squared value is subtracted from the reference signal v_{REF} to produce an amplitude error signal. Assuming that the radian frequency of the input signal is ω, the peak amplitude of the signal v_3 is A, and the sampling period is T, and the integer n designates the sampling index, then the input signal $v_3(n)$ can be expressed as:

$$v_3(n) = A \sin(\omega n T)$$

by applying a simple trigonometric identity, the square of the signal $v_3(n)$ is:

$$y(n) = v_3{}^2(n) = A^2 [\sin(\omega n T)]^2 = 0.5 A^2 - 0.5 A^2 \cos(2\omega n T)]$$

Therefore, the squared signal, $y(n)$, consists of two components; a zero-frequency signal information about the amplitude of the signal, $0.5 A^2$; plus a single (unknown)-frequency sinusoid, $-0.5 A^2 \cos(2\omega n T)$.

The reference signal V_{REF} sets the amplitude of the signal v_3. If the desired signal amplitude is D, and the value V_{REF} is a constant, then V_{REF} should have a value of $0.5 D^2$. A subtractor 327 subtracts the square from the multiplier 326 from V_{REF}, so that the different signal x_n has a DC value of $0.5(D^2-A^2)$, plus the double frequency term containing 2ω. The zero-frequency error signal $0.5(D^2-A^2)$ is produced even though none of the sample values of the signal v_3 may have a value equal to the amplitude A.

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In order to remove the double frequency term, the automatic gain control 146 includes a notch filter generally designated 328. This notch filter includes a first delay unit 329 producing a signal x_{n-1}, and a second delay unit 330 producing a signal x_{n-2}. The notch filter further includes a multiplier 331 for multiplying the signal x_{n-1} by a tuning parameter β_5, and an adder/subtractor 332 which adds the signal x_n to the signal x_{n-2} and subtracts the product from the multiplier 331 to produce an amplitude error signal v_{14} from which the double frequency term is substantially removed. The signal v_{14} is scaled by an adjustable scale factor μ_3 to produce a scaled error signal that is accumulated by the accumulator 322.

The tuning parameter β_5 sets the notch frequency for the notch filter 328. β_5 could be obtained by doubling β_1 of the tracking filter. Alternatively, as further shown in FIG. 23, a feedback loop automatically adjusts the tuning parameter β_5 in order to minimize the presence of the double frequency term in the signal v_{14}. In particular, this feedback loop includes a high-pass filter generally designated 333 for removing the DC component of the signal v_{14} to produce an error signal ϵ. The high-pass filter includes a delay unit 334 and a subtractor 335 which computes the difference between the signal v_{14} and the output of the delay unit 334.

In order to determine a signal for adjusting β_5 to minimize the double frequency component in the error signal ϵ, consider that the frequency response $F_1(z)$ of a notch filter 328 is:

$$F_1(z) = 1 - \beta_5 z^{-1} + z^{-2}$$

and the frequency response of $F_2(z)$ of the high-pass filter 333 is:

$$F_2(z) = 1 - z^{-1}$$

Therefore, the combined transfer function of the notch filter and the high-pass filter is:

$$F_1(z)F_2(z) = 1 - (1+\beta_5)z^{-1} + (1+\beta_5)z^{-2} - z^{-3}$$

and the error signal ϵ as given by:

$$\epsilon = x_n - (1+\beta_5)x_{n-1} + (1+\beta_5)x_{n-2} - x_{n-3}$$

The rate of change of the error signal ϵ with respect to the tuning parameter β_5 is:

$$\partial\epsilon/\partial\beta_5 = -x_{n-1} + x_{n-2}$$

What is desired is to determine the rate of change of the tuning signal β_5 with respect to time ($\dot{\beta}_5$) in order to minimize a performance index $J = \epsilon^2$ by making the rate of change of β_5 proportional to the error, i.e., $\dot{\beta}_5 = -\partial J/\partial\beta_5 \mu_4$ where μ_4 is a convergence parameter. First note that the rate of change of J with respect to β_5 is given by:

$$\partial J/\partial\beta_5 = (\partial J/\partial\epsilon)(\partial\epsilon/\partial\beta_5)$$

and the rate of change of J with respect to ϵ is given by:

$$\partial J/\partial\epsilon = 2\epsilon$$

Therefore, the desired solution is:

$$\dot{\beta}_5 = \Delta\beta_5/T = -\mu_4(\partial J/\partial\beta_5) = -\mu_4(\partial J/\partial\epsilon)(\partial\epsilon/\partial\beta_5)$$
$$\dot{\beta}_5 = -2\mu_4\epsilon(-x_{n-1} + x_{n-2})$$

In order to compute the desired control parameter $\dot{\beta}_5$, a subtractor 336 subtracts x_{n-2} from x_{n-1} to produce a signal indicating the rate of change of ϵ with respect to β_5. A multiplier 337 multiplies this difference from the subtractor 336 with ϵ from the subtractor 335 and further multiplies this product by a preselected coefficient $2\mu_4$ to produce the desired control parameter $\dot{\beta}_5$. In effect, the multiplier 337 multiplies the derivative $(x_{n-1} - x_{n-2})$ of the notch filter input signal x by the derivative of the notch filter output signal v_{14} to produce the tuning control parameter $\dot{\beta}_5$. The control parameter $\dot{\beta}_5$ is accumulated in an accumulator generally designated 338 including an adder 339, a limiter 340, and a delay unit or accumulator register

341. The delay unit 341 provides the tuning parameter β_5. The accumulator 328 functions as an integrator and lowpass filter.

Turning now to FIG. 24, there is shown a schematic diagram of the test oscillator 253. The test signal S_T is the output of a delay unit or register 351 providing a delay of one sampling period T. The test signal S_T is fed back to another delay unit or register 352 also providing a delay of one sampling period T, and scaled in a scaling unit 353 having a gain set to $2\cos\omega_1 T$. This gain of the scaling unit 353 determines the frequency ω_1 of the test signal S_T. A subtractor 354 subtracts the output of the scaling unit 353 from the output S_T' of the delay unit 352 to produce a sum that is received by the delay unit 351. Initially, the delay unit 352 is set to a value of zero, and the delay unit 351 is set to a value of $\sin\omega_1 T$. The tuning parameter β_4 is equal to $2\cos(2\omega_1 T)$. These initial conditions (IC), for example, are preset values that are initially loaded into the registers or memory locations of the delay units 351, 352 when the inertial measurement unit 50 of FIG. 1 is first turned on.

Turning now to FIG. 25, there is shown a flowchart 360 of a procedure for selectively resetting the test oscillator (253 in FIG. 24) from time-to-time to prevent amplitude drift in the test signal S_T due to accumulation of roundoff error. The procedure of FIG. 25, for example, is performed once during each sampling time. When the synchronous logic of FIG. 14 is implemented as a programmed digital signal processor, for example, the procedure of FIG. 25 is specified by a routine performed when the processor is interrupted at the sampling frequency f_s.

In the first step 361, the value of the output S_T' of the delay unit 352 is compared to zero. If it is not zero, then no resetting of the oscillator is performed for the sampling time. Otherwise, if the value of S_T' is equal to zero, then in step 362, the value of the test signal S_T from the delay unit 351 is compared to zero. If the value of the test signal S_T from the delay unit 351 is less than zero, then in step 363 the delay unit 351 in FIG. 24 is reset in order to set the value of the test signal S_T to a value of $-\sin\omega_1 T$. Otherwise, in step 364, when the value of the test signal S_T is greater than zero, the delay unit 351 in FIG. 24 is reset in order to set the value of the test signal S_T to a value of $\sin\omega_1 T$.

In view of the above, there has been described a digital tracking filter that can automatically adjust its bandwidth and center frequency to acquire and track a sinusoidal signal that drifts in frequency. Because the tracking filter generates in-phase and quadrature-phase reference signals by a Hilbert transform of the filtered output signal, the acquisition range of the filter is extremely wide, and the acquisition time is very short. Because the tracking filter automatically adjusts it bandwidth, it has very good noise rejection capabilities despite its wide acquisition range.

<u>APPENDIX I</u>

MATHCAD (Trademark) PROGRAM
TRACKING FILTER DESIGN
QRSTRACK
****

INPUTS

$f_s := 2^{15}$ $f_s = 3.277 \ 10^4$

The sampling frequency in Hz.

$f_b := 500$

The 3-dB-passband width of the filter in Hz.

$f_o := 10000$

Tuning frequency of the filter. The actual adjustment is via parameter β.

$N := 1$

Number of cascaded stages of filtering.

****

SETUP

$T := f_s^{-1}$

Sampling period: $T = 3.052 \ 10^{-5}$

$\alpha := \dfrac{1 - \tan [0.5 \pi \cdot f_b \cdot T]}{1 + \tan [[0.5 \pi \cdot f_b \cdot T]]}$

The passband-width parameter:
$\alpha = 0.953$

$\beta := -\cos [2 \pi \cdot f_o \cdot T]$

The tuning parameter: $\beta = 0.34$

$K := 100$ $k := 0 .. K - 1$

The number of frequency-analysis points used in performance evaluation and the frequency-analysis index.

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$$f_k := \frac{f_s}{2} \cdot \frac{k + 1}{K}$$

The analysis frequencies.

$$z := \overline{\exp(2j\pi \cdot f \cdot T)}$$

The discrete-time variable in steady state.

$$G := \overline{\left[\frac{z^{-2} + \beta \cdot (1 + \alpha) \cdot z^{-1} + \alpha}{1 + \beta \cdot (1 + \alpha) \cdot z^{-1} + \alpha \cdot z^{-2}}\right]}$$

The simplest second-order all-pass filter realizable by a Gray-Markel lattice structure.

$$H := \overline{\left[\left[\frac{1}{2} \cdot (1 - G)\right]^N\right]}$$

A simple 2nd-order bandpass filter with unity passband gain, single-parameter tuning, single-parameter passband-width adjustment, and minimum coefficient sensitivity.

$$HdB := 20 \cdot \overline{\log(H)}$$

Filter amplitude-frequency response expressed in dB.

$$R := \overline{\left[\frac{Im(H)}{Re(H)}\right]}$$

The Q/I ratio of Hilbert-transform outputs.

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APPENDIX II.

MATHCAD (Trademark) PROGRAM
OPTIMUM HILBERT TRANSFORMER DESIGN PROGRAM
QRSHILBERT.MCD

****

INITIALIZE

$f_s := 2^{15}$

Sampling frequency

$f_{min} := 8000$

Minimum Hilbert transformer passband edge

$f_{max} := 12000$

Maximum Hilbert transformer passband edge

$f_0 := f_{max} - \dfrac{f_s}{4} \qquad f_1 := \dfrac{f_s}{4} - f_{min}$

Frequency vector components

$R := \dfrac{f_s}{max(f)} \qquad R = 8.605$

Ratio of sampling frequency to passband-edge frequency of the baseband filter

$B := 30$

Number of bits to use in coefficient values

$A_{pb} := -90$

Passband peak ripple spec in dB

$N := floor\left[R \cdot \dfrac{A_{pb} + 13}{29.2 \cdot (4 - R)} + \dfrac{1}{4} \right]$

Calculation of number of multiplier coefficients required to meet the ripple spec.

$m := 0 ..N \qquad\qquad ZERO_m := 0 \qquad\qquad N = 5$

WRITEPRN(FB) := ZERO □   PRINTCOLWIDTH := 10

WRITEPRN(FA) := ZERO □   PRNPRECISION := 10

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WRITE(COUNT) := 0 □   Type "PROCESS", comment FA, FB, & COUNT, then GOTO 165.

****

SETUP

ITERATION := READ(COUNT)	ITERATION = 3	PBE := $(R)^{-1}$
WRITE(COUNT) := 1 + ITERATION		PBE = passband edge
ITERATION := READ(COUNT)	ITERATION = 4	PBE = 0.1162109375

$n := 0 .. N$

$q := 0 .. N - 1$

n and r are indices. "N" is reserved for computing the filter performance error or ripple; index values 0 through N-1 are for the actual multiplier-coefficient indices. The multiplier-coefficient index is q.

FA := READPRN(FA)

Measured passband extremal frequencies

FB := READPRN(FB)

Measured stopband extremal frequencies

$$FPB_m := if\left[ITERATION = 1, PBE \cdot \frac{m}{N}, FA_m\right]$$

Passband extremal frequencies used in calculations

$$FSB_m := if\left[ITERATION = 1, \frac{1}{2} - \left[1 - \frac{m}{N}\right] \cdot PBE, FB_m\right]$$

Stopband extremal frequencies used in calculations.

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$$M_{m,n} := if\left[n = N, 2\cdot(-1)^m, 4\cdot cos\left[(2\cdot n + 1)\cdot 2\cdot \pi\cdot FPB_m\right]\right]$$

Remez matrix

$$r_m := 1$$

The all-unit vector.

$$\alpha := M^{-1}\cdot r$$

The coefficient and error vector.

$$\delta := \alpha_N$$

The error measure

$$a_q := 2^{-B}\cdot\left[floor\left[.5 + 2^{B+1}\cdot\alpha_q\right]\right]$$

Filter coefficients doubled and rounded to B bits.

$$K := 256$$

Number of points for frequency analysis.

$$k := 0..K - 1$$

Frequency-response evaluation index.

$$FFPB_k := PBE\cdot\frac{k}{K - 1}$$

Frequency variable for passband-performance evaluation.

$$FFSB := \frac{1}{2} - FFPB$$

Frequency variables for stopband-performance evaluation.

$$FG := \frac{1}{2}\cdot\frac{FFPB}{PBE}$$

Frequency variable for total filter evaluation.

****

PASSBAND PERFORMANCE EVALUATION

The exact expression for the passband error is:

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$$EPB := 1 - \frac{1}{2} \cdot \left[1 + \sum_q 2 \cdot a_q \cdot \cos\left(\left(2 \cdot q + 1\right) \cdot 2 \cdot \pi \cdot FFPB\right) \right]$$

$EPB_K := EPB_{K-1}$

Define an artificial end point to make the notation work.

$XPB_{k+1} := if\left[EPB_{k+1} < EPB_k, \delta, -\delta\right]$

Filter performance and passband extremal-frequency marker.

Now we can estimate the passband extremal frequencies:

$PB_{k+1} := if\left[XPB_{k+1} = -XPB_k, FFPB_k, PBE\right]$

$SPB_m := (sort(PB))_m$

Extract $N + 1$ passband extremal-frequency estimates.

$WRITEPRN(FA) := SPB$

This puts the estimated passband extremal frequencies into memory.

$PBRIPPLE := 20 \cdot \log\left[\max\left(\left(\left|EPB\right|\right)\right)\right]$

Computation of the peak passband ripple dB.

* *

STOPBAND PERFORMANCE EVALUATION

The exact expression for the stopband error is:

$$ESB := 0 - \frac{1}{2} \cdot \left[1 + \sum_q 2 \cdot a_q \cdot \cos\left(\left(2 \cdot q + 1\right) \cdot 2 \cdot \pi \cdot FFSB\right) \right]$$

$ESB_K := ESB_{K-1}$

Define an artificial end point to make the notation work.

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$$XSB_{k+1} := if \left[ESB_{k+1} < ESB_k, -\delta, \delta \right]$$

Filter performance and stopband extremal-frequency marker.

Now we can estimate the stopband extremal frequencies:

$$SB_{k+1} := if \left[XSB_{k+1} = -XSB_k, FFSB_k, \frac{1}{2} - PBE \right] \qquad SB_K := \frac{1}{2}$$

$$SORTSB_m := (-sort(-SB))_m$$

$$SSB := sort(SORTSB)$$

Extract N + 1 stopband extremal-frequency estimates and sort them in ascending order.

$$WRITEPRN(FB) := SSB$$

This puts the estimated stopband extremal frequencies into memory.

$$SBRIPPLE := 20 \cdot log \left[max \left[(|ESB|) \right] \right]$$

Compute the peak stopband ripple in dB.

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PROTOTYPE FILTER PERFORMANCE SUMMARY

The cascaded half-band prototype filter overall frequency response is given by:

$$GPB := \frac{1}{2} \cdot \left[1 + \sum_q 2 \cdot a_q \cdot \cos((2 \cdot q + 1) \cdot 2 \cdot \pi \cdot FG) \right]$$

Filter coefficient values:

$$a = \begin{bmatrix} 0.6142410357 \\ -0.1529612327 \\ 0.0496214228 \\ 0.0127215311 \\ 0.0018368168 \end{bmatrix}$$

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ITERATION = 4   N = 5
PBRIPPLE = -95.6   B = 30
SBRIPPLE = -95.6   R = 8.6050420168
SPECS: A_{pb} = -90 δ = -0.000016511

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CONVERT THE PROTOTYPE DESIGN TO A HILBERT TRANSFORMER

$$FH_k := \frac{k}{K}$$

The evaluation frequencies

$$j := \sqrt{-1}$$

Discrete-time variable in steady state

$$z := \overline{\exp(j \cdot 2 \cdot \pi \cdot FH)}$$

$$p := 0.44 \cdot N - 2$$

Hilbert-transformer-coefficient index

A useful auxiliary vector

$$i_p := p - (2 \cdot N - 1)$$

The Hilbert transformer coefficient values:

$$b_p := if\left[p = 2 \cdot N - 1, 1, if\left[\mod(p, 2) = 1, 0, a_{\left[\frac{|i_p|-1}{2}\right]}\right]\right] \cdot \exp\left[j \cdot i_p \cdot \frac{\pi}{2}\right]$$

$$G := \left[z^{2 \cdot N - 1} \cdot \sum_p b_p \cdot z^{-p}\right]$$

The transfer function of the Hilbert transformer

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EVALUATE THE PERFORMANCE OF THE HILBERT TRANSFORMER

$$GR := \left| z^{2 \cdot N - 1} \cdot \sum_q Re[b_p] \cdot z^{-p} \right|$$

The real part of the Hilbert transformer

$$GI := \left| z^{2 \cdot N - 1} \cdot \sum_p Im[b_p] \cdot z^{-p} \right|$$

The imaginary part of the Hilbert transformer

$$b = \begin{bmatrix} -0.0018368168j \\ 0 \\ -0.0127215311j \\ 0 \\ -0.0496214228j \\ 0 \\ 0.1529612327j \\ 0 \\ 0.6142410357j \\ 1 \\ 0.6142410357j \\ 0 \\ 0.1529612327j \\ 0 \\ 0.0496214228j \\ 0 \\ 0.0127215311j \\ 0 \\ 0.0018368168j \end{bmatrix}$$

END OF PROGRAM

The invention may be summarized as follows:

1. A method of filtering an input signal, said method comprising the steps of:

(a) passing said input signal through an adjustable filter having an adjustable passband center frequency to produce a filtered signal;

(b) producing an in-phase reference signal and a quadrature-phase reference signal from said filtered signal;

(c) demodulating said input signal with said in-phase reference signal and said quadrature-phase reference signal to produce a frequency-control signal; and

(d) adjusting said passband center frequency of said adjustable filter in response to said frequency-control signal.

2. The method, wherein said quadrature-phase reference signal is produced in said step (b) by a Hilbert transform of said filtered signal.

3. The method, wherein said adjustable filter has an adjustable passband-width, and wherein said method includes adjusting said passband-width of said adjustable filter in proportion to absolute value of a rate of change of said frequency-control signal.

4. The method, wherein said step (c) is performed by demodulating said input signal by said in-phase reference signal to produce an in-phase demodulated signal, demodulating said input signal by said quadrature-phase reference signal to produce a quadrature-phase demodulated signal, filtering said in-phase demodulated signal to produce a filtered in-phase demodulated signal, filtering said quadrature-phase demodulated signal to produce a filtered quadrature-phase demodulated signal, dividing said filtered quadrature-phase demodulated signal by said filtered in-phase demodulated signal to produce a quotient signal, and integrating said quotient signal to produce said frequency-control signal.

5. The method, wherein said demodulated in-phase signal is filtered in a first adjustable notch filter having an adjustable passband center frequency, and said demodulated quadrature-phase signal is filtered in a second adjustable notch filter having an adjustable passband center frequency, and wherein said method further includes adjusting said passband center frequencies of said adjustable notch filters in response to said frequency-control signal.

6. The method, wherein said adjustable filter has an adjustable passband width, and wherein said method further includes producing a passband-width control signal in response to absolute value of said quotient signal, and adjusting said passband width in response to said passband-width control signal.

7. The method, wherein said demodulated in-phase signal is filtered in a first adjustable notch filter having an adjustable passband center frequency and an adjustable passband width, and said demodulated quadrature-phase signal is filtered in a second adjustable notch filter having an adjustable center frequency and an adjustable passband width, and wherein said method further includes adjusting said passband center frequencies of said adjustable notch filters in response to said frequency control signal, and adjusting said passband widths of said adjustable notch filters in response to said passband-width control signal.

8. A tracking filter comprising:

(a) a tunable filter responsive to an input signal for producing a filtered signal on an output, said tunable filter having an adjustable passband center frequency responsive to a frequency control signal;

(c) a reference signal generator having an input connected to said output for producing an in-phase reference signal and a quadrature-phase reference signal in response to said filtered signal; and

(b) a frequency discriminator responsive to said input signal and connected to said reference signal generator and said tunable filter for producing said frequency control signal by complex demodulation of said input signal with said in-phase reference signal and said quadrature-phase reference signal.

9. The tracking filter, wherein said reference signal generator is a Hilbert transformer.

10. The tracking filter, wherein said tunable filter is responsive to a passband-width control signal, and said frequency discriminator includes means for generating said passband-width control signal.

11. The tracking filter, wherein said means for generating said passband-width control signal includes means for determining a magnitude of a difference between frequency of said input signal and frequency of said in-phase reference signal so that said tunable filter has a passband width of at least twice the difference between said frequency of said input signal and said frequency of said in-phase reference signal.

12. The tracking filter, wherein said frequency discriminator includes a first multiplier for multiplying said in-phase reference signal by said input signal to produce an in-phase product signal, a second multiplier for multiplying said quadrature-phase reference signal by said input signal to produce a quadrature-phase product signal, a first lowpass filter connected to said first multiplier for filtering said in-phase product signal to produce a filtered in-phase product signal, a second lowpass filter connected to said second multiplier for filtering said quadrature-phase product signal to produce a filtered quadrature-phase product signal, a divider connected to said first lowpass filter and said second lowpass filter for dividing said filtered quadrature-phase product signal by said filtered in-phase product signal to produce a quotient signal, and an integrator connected to said divider for integrating said quotient signal to produce said frequency control signal.

13. The tracking filter, wherein said tunable filter is responsive to a passband-width control signal, and said frequency discriminator includes an absolute value unit connected to said divider for producing said passband-width control signal so that said tunable filter has a passband width that is adjusted in response to absolute value of said quotient signal of said divider unit.

14. The tracking filter, wherein said frequency discriminator includes a first adjustable notch filter connected between said first multiplier and said divider for notch filtering said in-phase product signal,

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and a second adjustable notch filter connected between said second multiplier and said divider for notch filtering said quadrature-phase product signal, and wherein each of said first adjustable notch filter and said second adjustable notch filter has a frequency control input connected to said integrator for receiving said frequency control signal.

15. The tracking filter, wherein each of said first adjustable notch filter and said second adjustable notch filter has a passband-width control input, and said frequency discriminator includes an absolute value unit connected to said divider for producing said passband-width control signal so that each of said first adjustable notch filter and said second adjustable notch filter has a passband width that is adjusted in response to absolute value of said quotient signal.

16. The tracking filter, wherein said tunable filter has a passband-width control input connected to said absolute value unit of said frequency discriminator for adjusting passband width of said tunable filter in response to absolute value of said quotient signal.

17. The tracking filter, wherein said tracking filter is a digital filter.

18. A tracking filter comprising:

(a) a tunable filter responsive to an input signal for producing a filtered signal on an output, said tunable filter having an adjustable passband center frequency responsive to a frequency control signal, said tunable filter having an adjustable passband width responsive to a passband-width control signal;

(c) a Hilbert transformer having an input connected to said output for producing an in-phase reference signal and a quadrature-phase reference signal in response to said filtered signal; and

(b) a frequency discriminator responsive to said input signal and connected to said Hilbert transformer and said tunable filter for producing said frequency control signal and said passband-width control signal by complex demodulation of said input signal with said in-phase reference signal and said quadrature-phase reference signal.

19. The tracking filter, wherein said frequency discriminator includes a first multiplier for multiplying said in-phase reference signal by said input signal to produce an in-phase product signal, a second multiplier for multiplying said quadrature-phase reference signal by said input signal to produce a quadrature-phase product signal, a first lowpass filter connected to said first multiplier for filtering said in-phase product signal to produce a filtered in-phase product signal, a second lowpass filter connected to said second multiplier for filtering said quadrature-phase product signal to produce a filtered quadrature-phase product signal, a divider connected to said first lowpass filter and said second lowpass filter for dividing said filtered quadrature-phase product signal by said filtered in-phase product signal to produce a quotient signal, an integrator connected to said divider for integrating said quotient signal to produce said frequency control signal, and an absolute value generator connected to said divider for producing said bandwidth control signal from an absolute value of said quotient signal.

20. The tracking filter, wherein said frequency discriminator includes a first adjustable notch filter connected between said first multiplier and said divider for notch filtering said in-phase product signal, and a second adjustable notch filter connected between said second multiplier and said divider for notch filtering said quadrature-phase product signal, and wherein each of said first adjustable notch filter and said second adjustable notch filter has a frequency control input connected to said integrator for receiving said frequency control signal, and a passband-width control input connected to said absolute value generator for receiving said passband-width control signal.

Claims

1. A method of filtering an input signal, said method comprising the steps of:

(a) passing said input signal through an adjustable filter having an adjustable passband center frequency to produce a filtered signal;

(b) producing an in-phase reference signal and a quadrature-phase reference signal from said filtered signal;

(c) demodulating said input signal with said in-phase reference signal and said quadrature-phase reference signal to produce a frequency-control signal; and

(d) adjusting said passband center frequency of said adjustable filter in response to said frequency-control signal.

2. The method as claimed in claim 1, wherein said quadrature-phase reference signal is produced in said step (b) by a Hilbert transform of said filtered signal.

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3. The method as claimed in claim 1, wherein said adjustable filter has an adjustable passband-width, and wherein said method includes adjusting said passband-width of said adjustable filter in proportion to absolute value of a rate of change of said frequency-control signal.

4. The method as claimed in claim 1, wherein said step (c) is performed by demodulating said input signal by said in-phase reference signal to produce an in-phase demodulated signal, demodulating said input signal by said quadrature-phase reference signal to produce a quadrature-phase demodulated signal, filtering said in-phase demodulated signal to produce a filtered in-phase demodulated signal, filtering said quadrature-phase demodulated signal to produce a filtered quadrature-phase demodulated signal, dividing said filtered quadrature-phase demodulated signal by said filtered in-phase demodulated signal to produce a quotient signal, and integrating said quotient signal to produce said frequency-control signal.

5. The method as claimed in claim 4, wherein said demodulated in-phase signal is filtered in a first adjustable notch filter having an adjustable passband center frequency, and said demodulated quadrature-phase signal is filtered in a second adjustable notch filter having an adjustable passband center frequency, and wherein said method further includes adjusting said passband center frequencies of said adjustable notch filters in response to said frequency-control signal,
   , **wherein preferably** said adjustable filter has an adjustable passband width, and wherein said method further includes producing a passband-width control signal in response to absolute value of said quotient signal, and adjusting said passband width in response to said passband-width control signal, **and**
   wherein preferably said demodulated in-phase signal is filtered in a first adjustable notch filter having an adjustable passband center frequency and an adjustable passband width, and said demodulated quadrature-phase signal is filtered in a second adjustable notch filter having an adjustable center frequency and an adjustable passband width, and wherein said method further includes adjusting said passband center frequencies of said adjustable notch filters in response to said frequency control signal, and adjusting said passband widths of said adjustable notch filters in response to said passband-width control signal.

6. A tracking filter comprising:
   (a) a tunable filter responsive to an input signal for producing a filtered signal on an output, said tunable filter having an adjustable passband center frequency responsive to a frequency control signal;
   (c) a reference signal generator having an input connected to said output for producing an in-phase reference signal and a quadrature-phase reference signal in response to said filtered signal; and
   (b) a frequency discriminator responsive to said input signal and connected to said reference signal generator and said tunable filter for producing said frequency control signal by complex demodulation of said input signal with said in-phase reference signal and said quadrature-phase reference signal.

7. The tracking filter as claimed in claim 6, wherein said reference signal generator is a Hilbert transformer,
   wherein said tunable filter is responsive to a passband-width control signal, and said frequency discriminator includes means for generating said passband-width control signal,
   wherein said means for generating said passband-width control signal includes means for determining a magnitude of a difference between frequency of said input signal and frequency of said in-phase reference signal so that said tunable filter has a passband width of at least twice the difference between said frequency of said input signal and said frequency of said in-phase reference signal,
   wherein said frequency discriminator includes a first multiplier for multiplying said in-phase reference signal by said input signal to produce an in-phase product signal, a second multiplier for multiplying said quadrature-phase reference signal by said input signal to produce a quadrature-phase product signal, a first lowpass filter connected to said first multiplier for filtering said in-phase product signal to produce a filtered in-phase product signal, a second lowpass filter connected to said second multiplier for filtering said quadrature-phase product signal to produce a filtered quadrature-phase product signal, a divider connected to said first lowpass filter and said second lowpass filter for dividing said filtered quadrature-phase product signal by said filtered in-phase product signal to produce a quotient signal, and an integrator connected to said divider for integrating said quotient signal to

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produce said frequency control signal,

wherein said tunable filter is responsive to a passband-width control signal, and said frequency discriminator includes an absolute value unit connected to said divider for producing said passband-width control signal so that said tunable filter has a passband width that is adjusted in response to absolute value of said quotient signal of said divider unit,

wherein said frequency discriminator includes a first adjustable notch filter connected between said first multiplier and said divider for notch filtering said in-phase product signal, and a second adjustable notch filter connected between said second multiplier and said divider for notch filtering said quadrature-phase product signal, and wherein each of said first adjustable notch filter and said second adjustable notch filter has a frequency control input connected to said integrator for receiving said frequency control signal,

wherein each of said first adjustable notch filter and said second adjustable notch filter has a passband-width control input, and said frequency discriminator includes an absolute value unit connected to said divider for producing said passband-width control signal so that each of said first adjustable notch filter and said second adjustable notch filter has a passband width that is adjusted in response to absolute value of said quotient signal,

wherein said tunable filter has a passband-width control input connected to said absolute value unit of said frequency discriminator for adjusting passband width of said tunable filter in response to absolute value of said quotient signal, and

wherein said tracking filter is a digital filter.

8. A tracking filter comprising:

(a) a tunable filter responsive to an input signal for producing a filtered signal on an output, said tunable filter having an adjustable passband center frequency responsive to a frequency control signal, said tunable filter having an adjustable passband width responsive to a passband-width control signal;

(c) a Hilbert transformer having an input connected to said output for producing an in-phase reference signal and a quadrature-phase reference signal in response to said filtered signal: and

(b) a frequency discriminator responsive to said input signal and connected to said Hilbert transformer and said tunable filter for producing said frequency control signal and said passband-width control signal by complex demodulation of said input signal with said in-phase reference signal and said quadrature-phase reference signal.

9. The tracking filter as claimed in claim 8, wherein said frequency discriminator includes a first multiplier for multiplying said in-phase reference signal by said input quadrature-phase product signal, and wherein each of said first adjustable notch filter and said second adjustable notch filter has a frequency control input connected to said integrator for receiving said frequency control signal, and a passband-width control input connected to said absolute value generator for receiving said passband-width control signal.

10. A method of filtering an input signal, said method comprising the steps of:

(a) passing said input signal through an adjustable filter to produce a filtered signal; and

(b) producing an in-phase reference signal and a quadratur-phase reference signal from said filtered signal.

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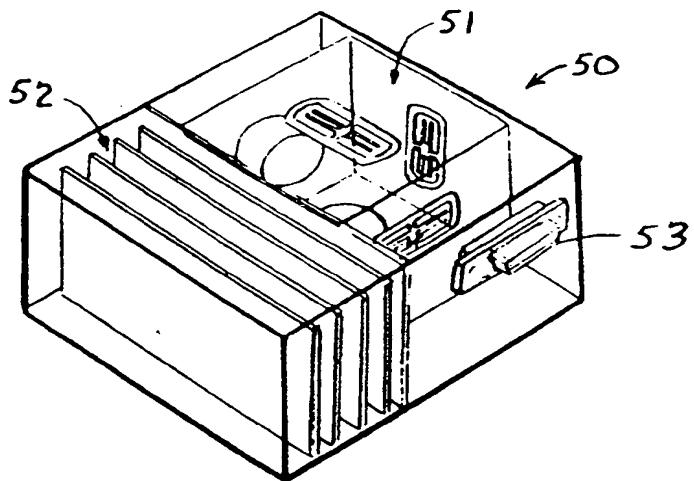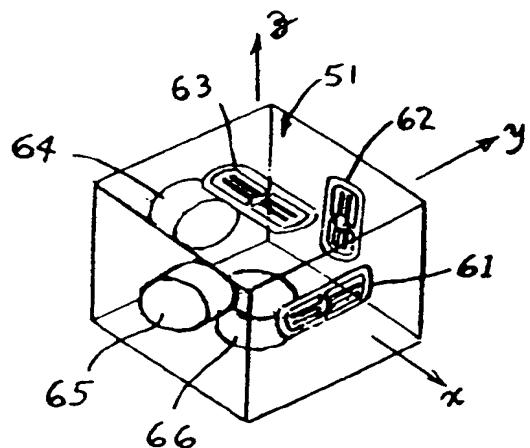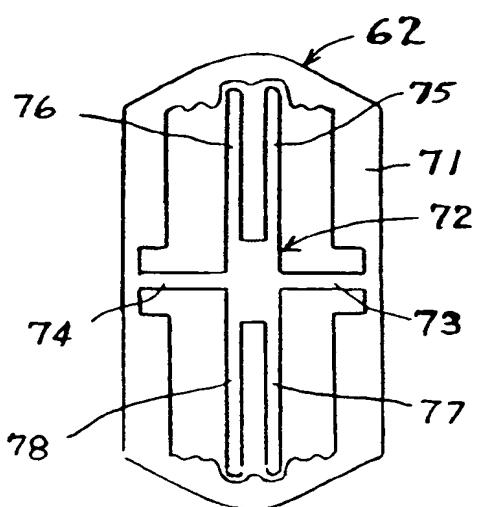
FIG. 1

FIG. 2

FIG. 3
(PRIOR ART)
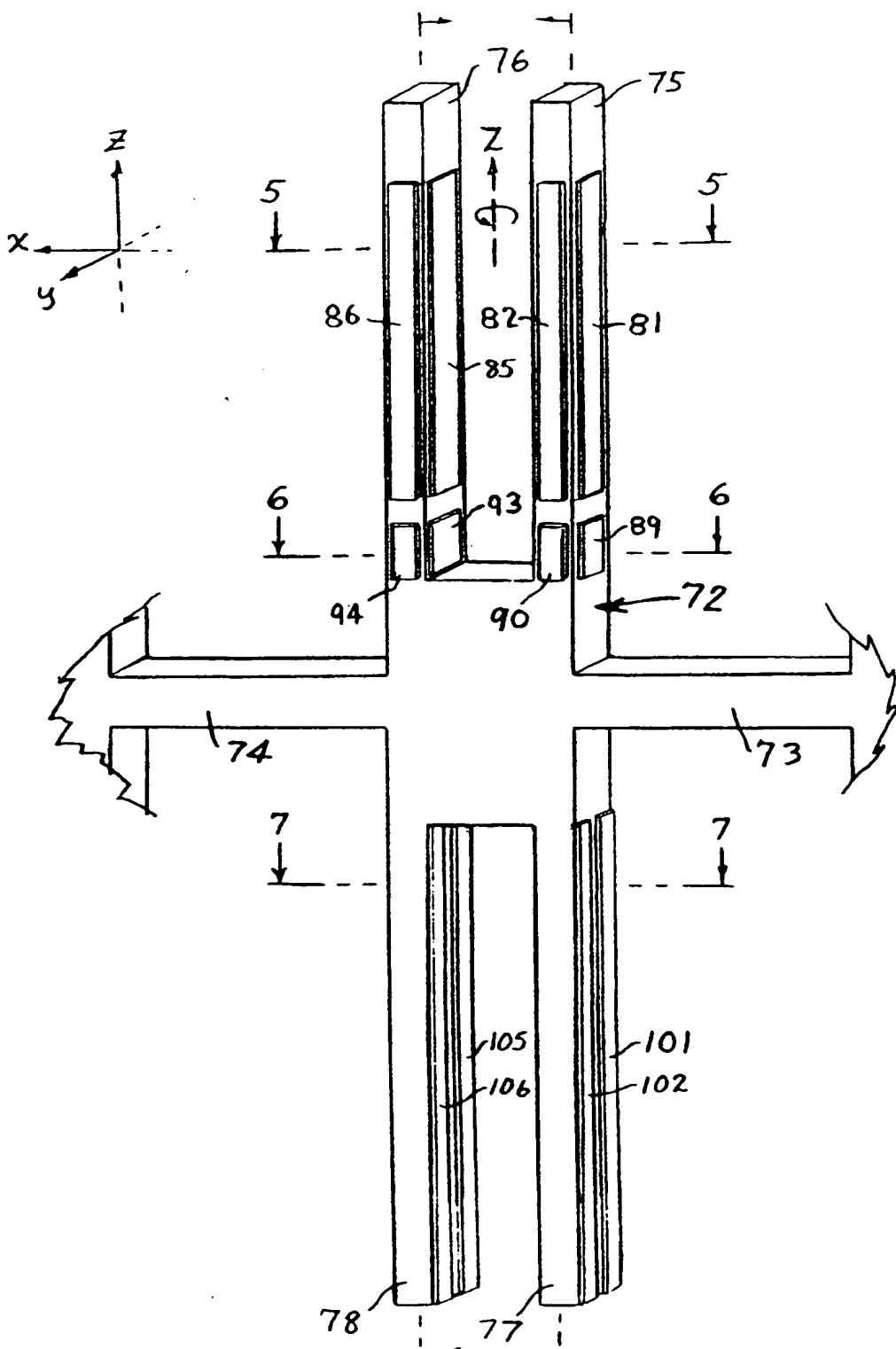
FIG. 4
(PRIOR ART)
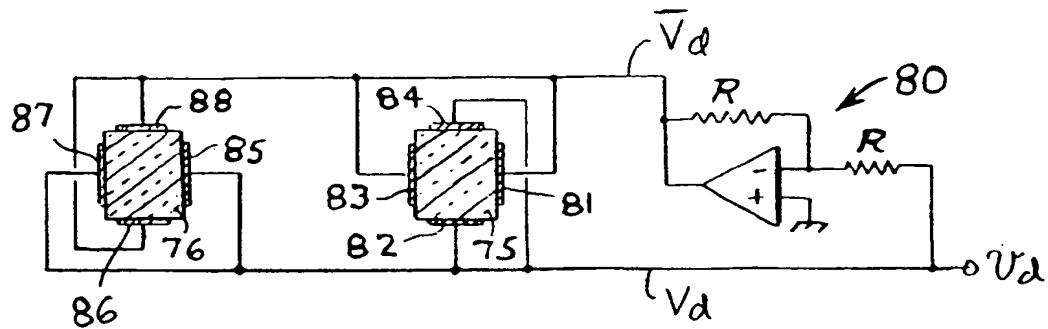
FIG. 5   (PRIOR ART)
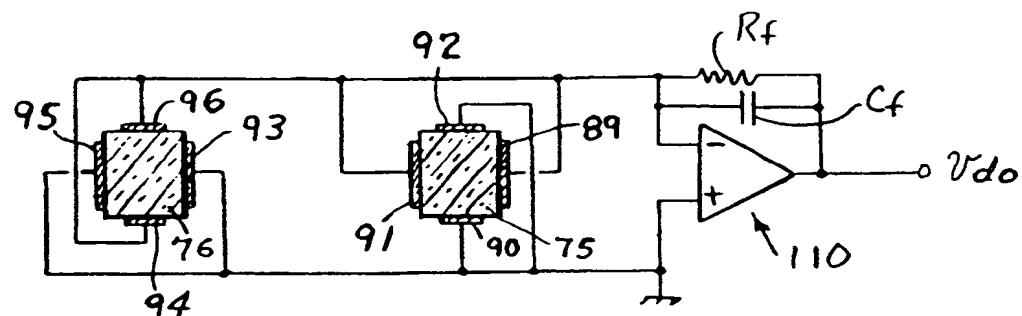
FIG. 6   (PRIOR ART)
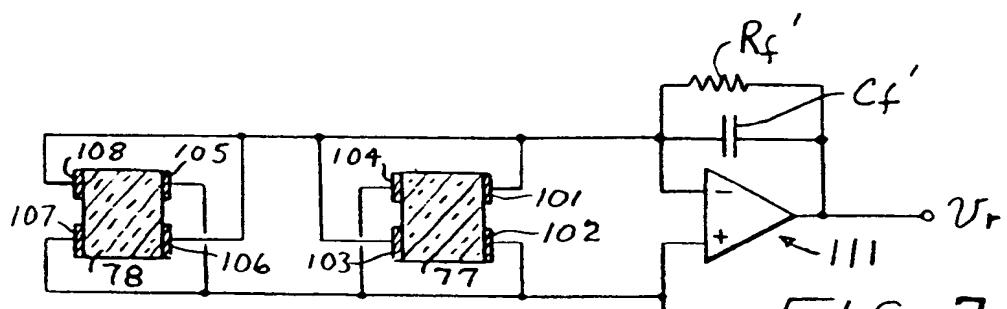
FIG. 7
(PRIOR ART)
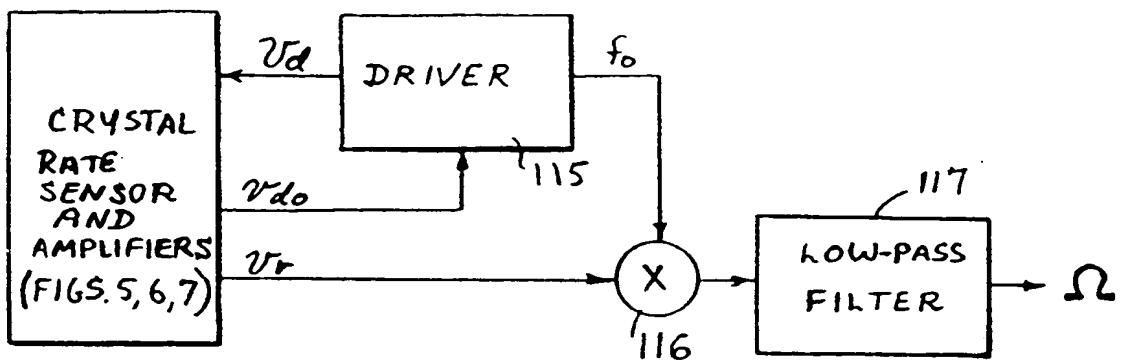
FIG. 8 (PRIOR ART)

FIG. 9
(PRIOR ART)

$-vd + vn$
$-vd - vn$
$vd - vn$
$vd + vn$

88a   88b
87b
87a
85a
85b
86b
76'
86a

84a   84b
83b   81a
83a   81b
82b   82a   75'

FIG. 10

(PRIOR ART)

R
R
$-vd + vn$
122
120

$-vd - vn$

R R vn
R
$vd - vn$
120
R
vd

R
R
$vd + vn$
R
123
121
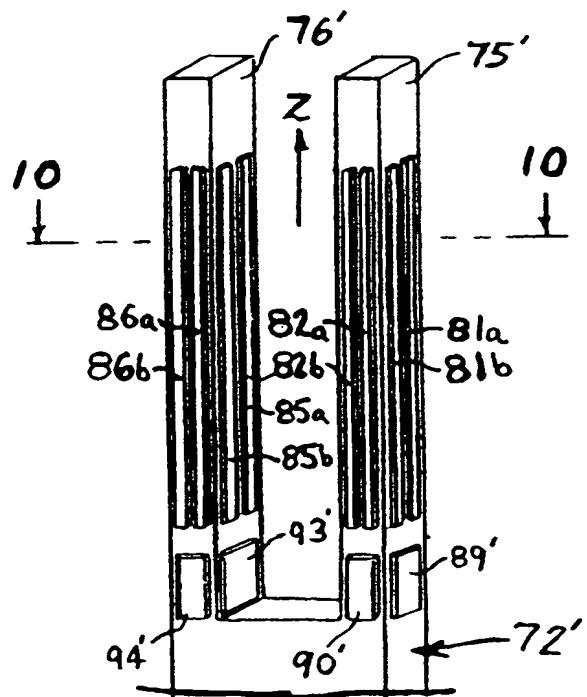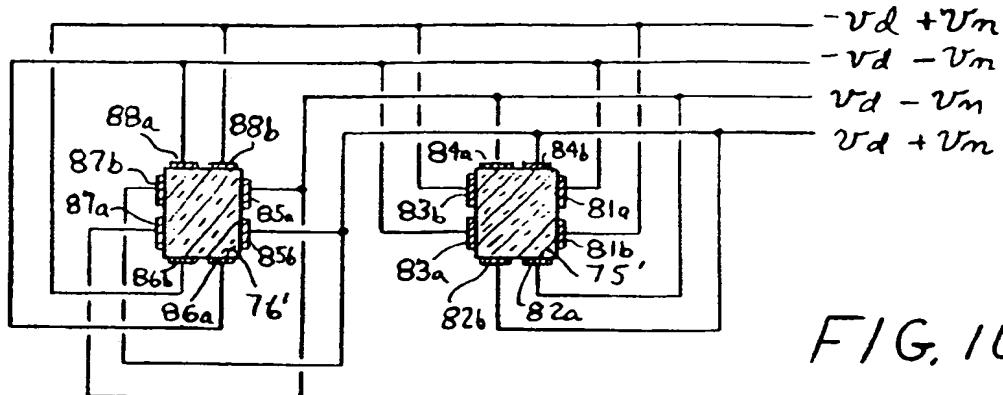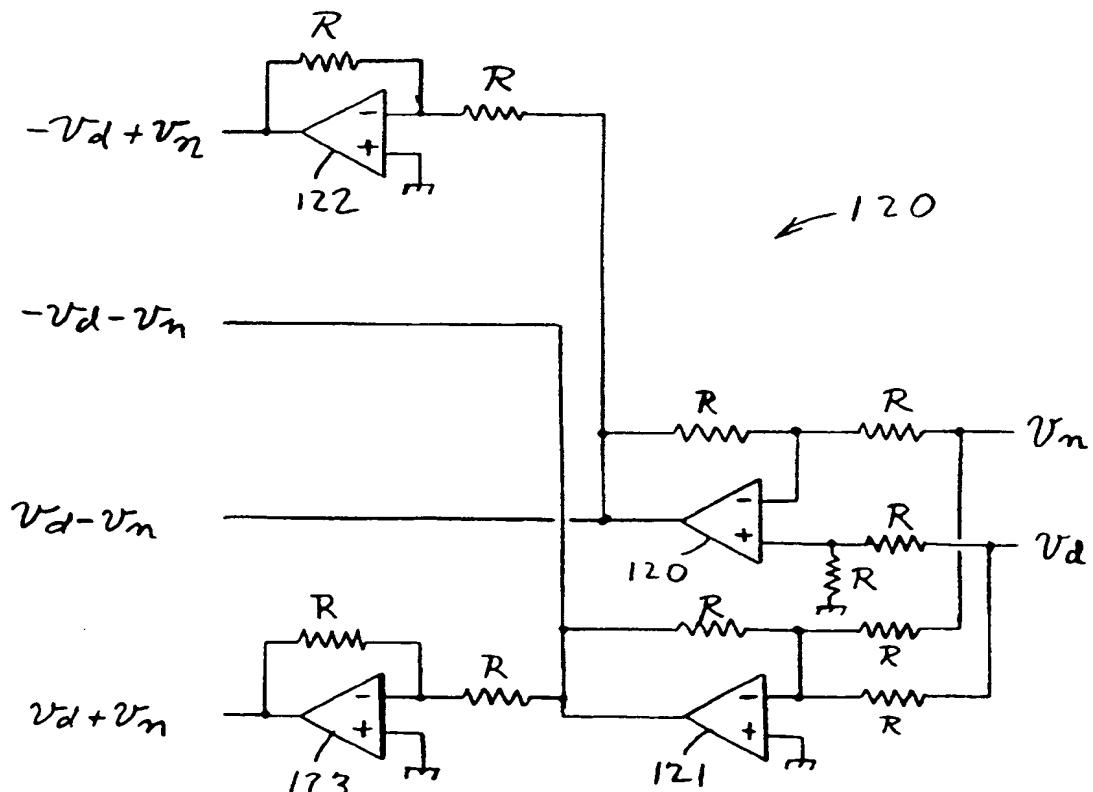
FIG. 11
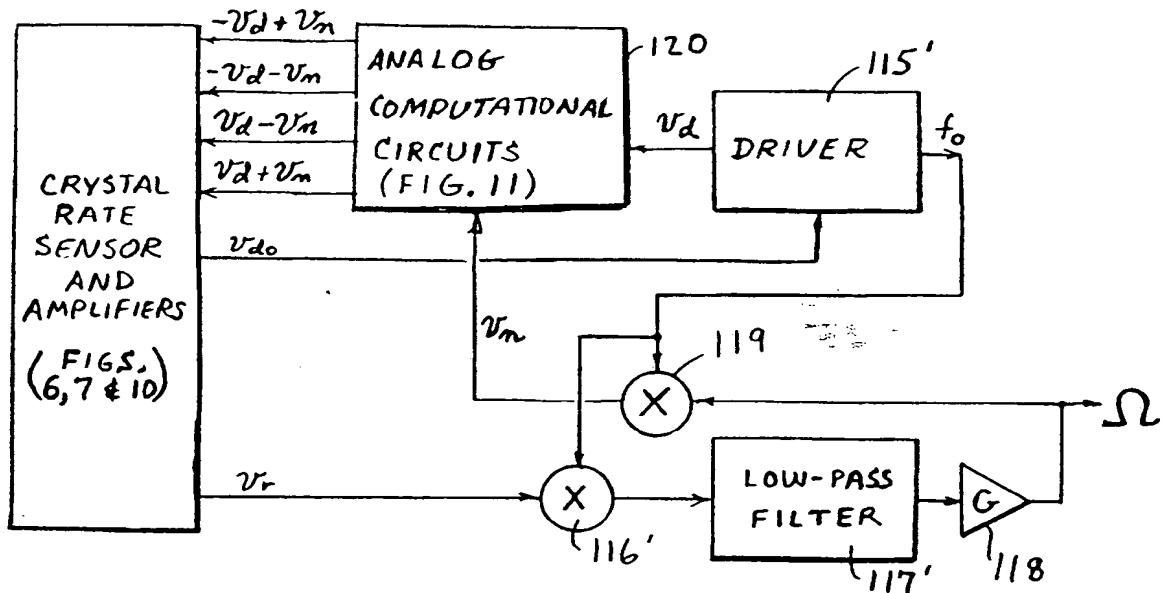
(PRIOR ART)

FIG. 12 (PRIOR ART)
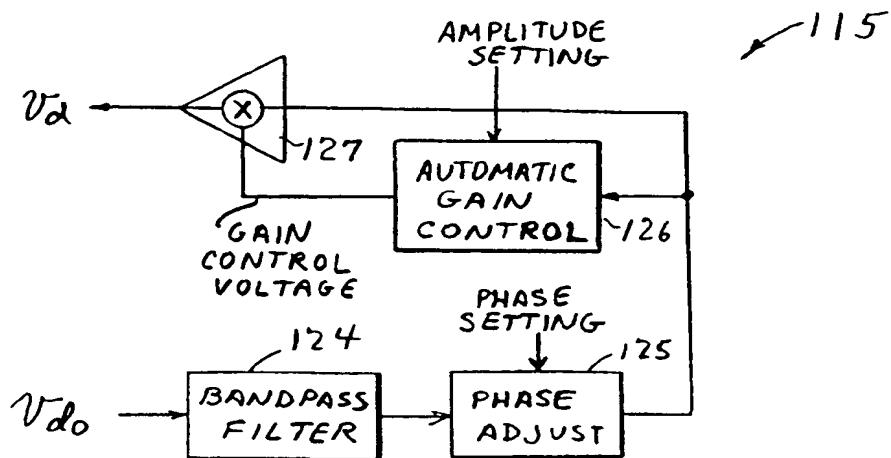
FIG. 13 (PRIOR ART)

FIG. 14

FIG. 15A

FIG. 15B
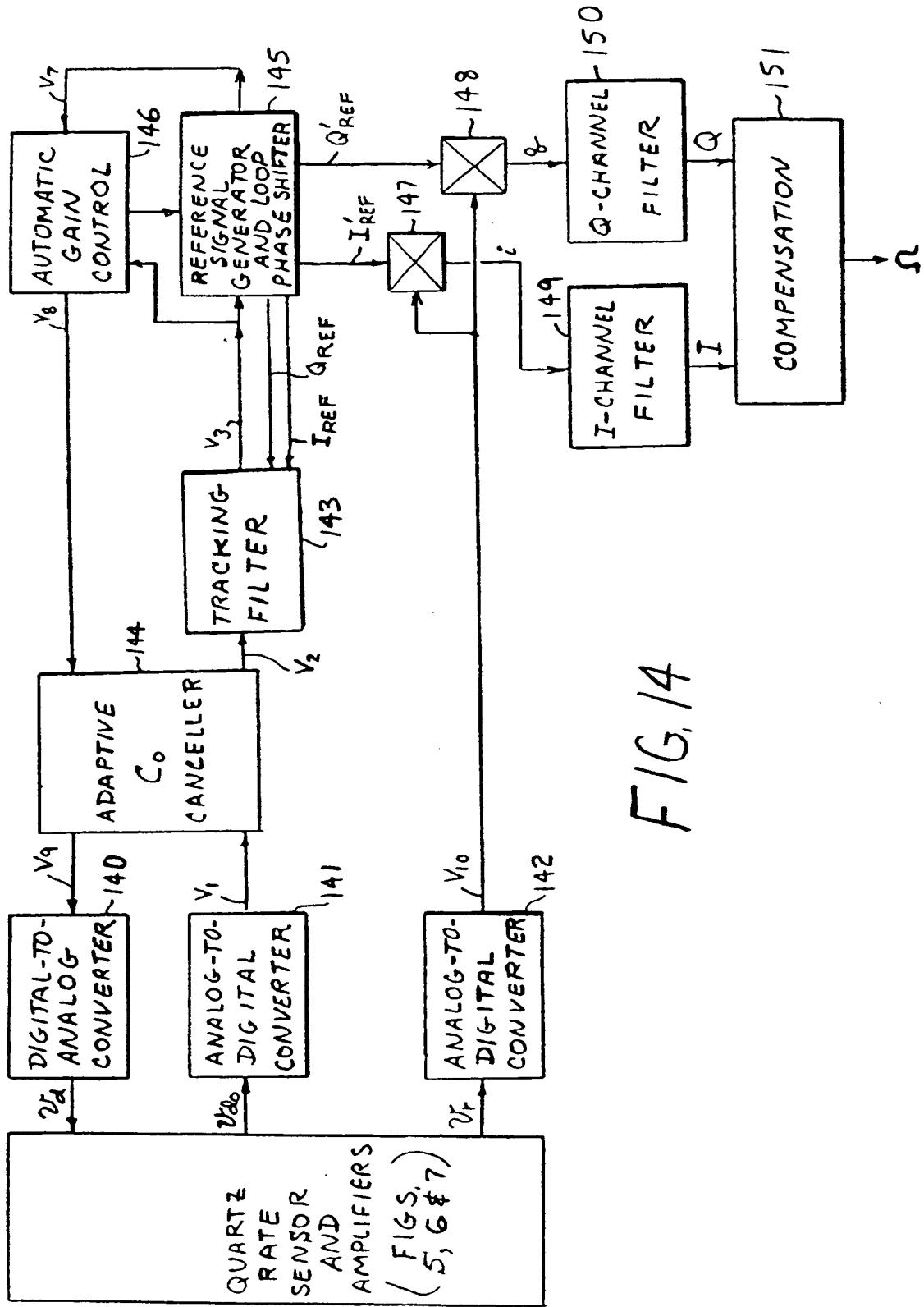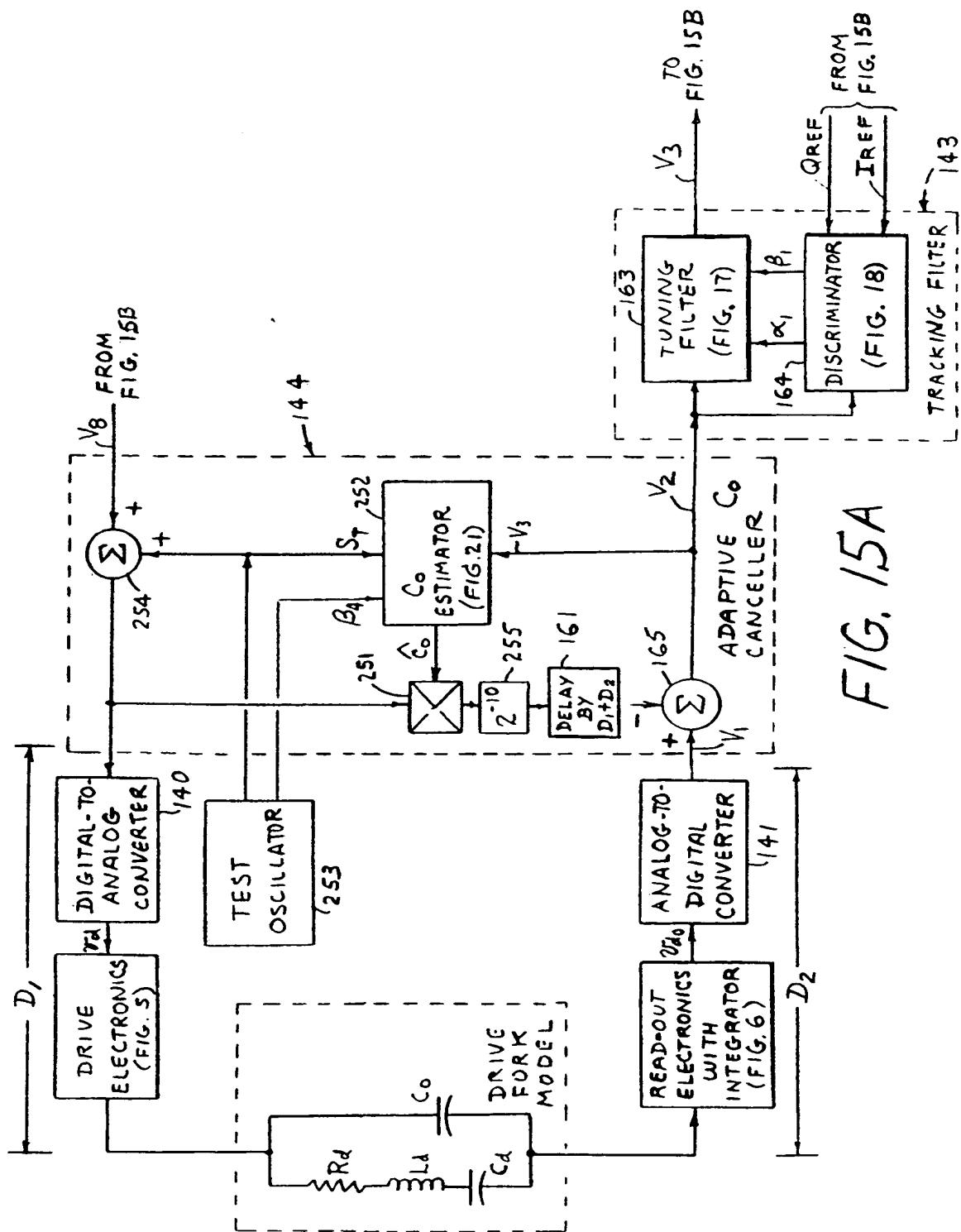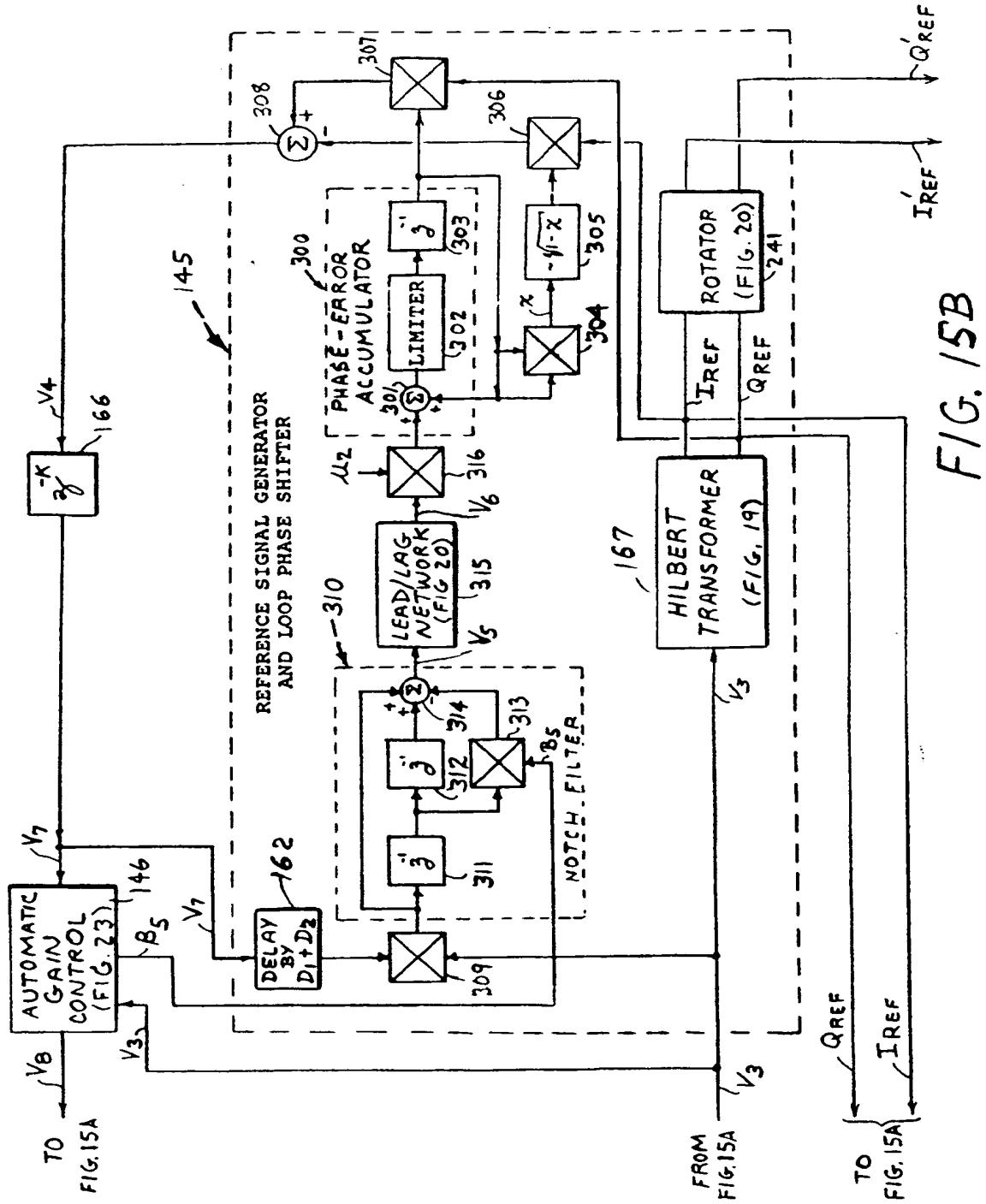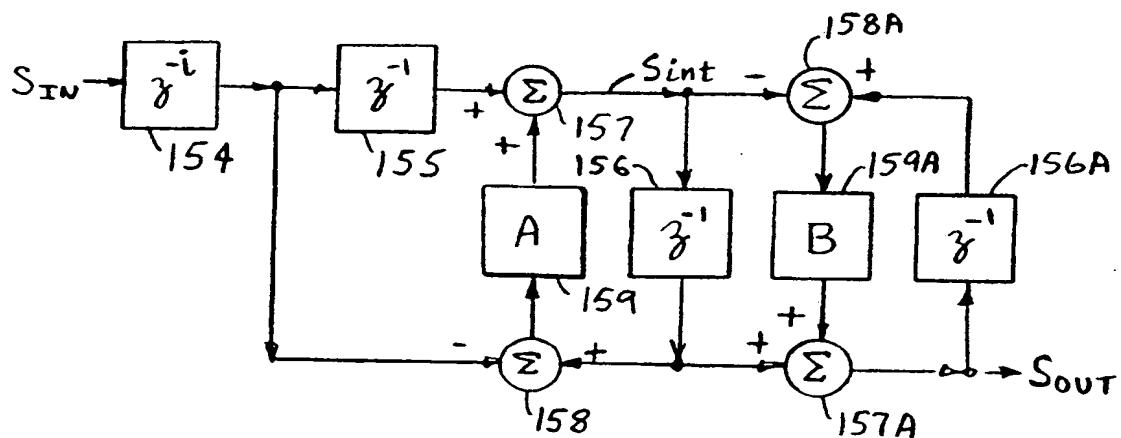
FIG. 16
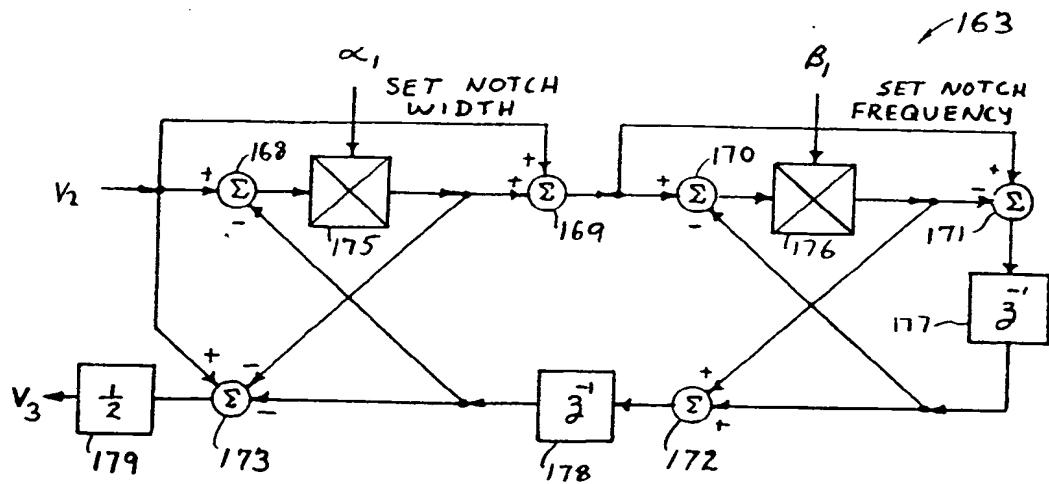
(PRIOR ART)   FIG. 17
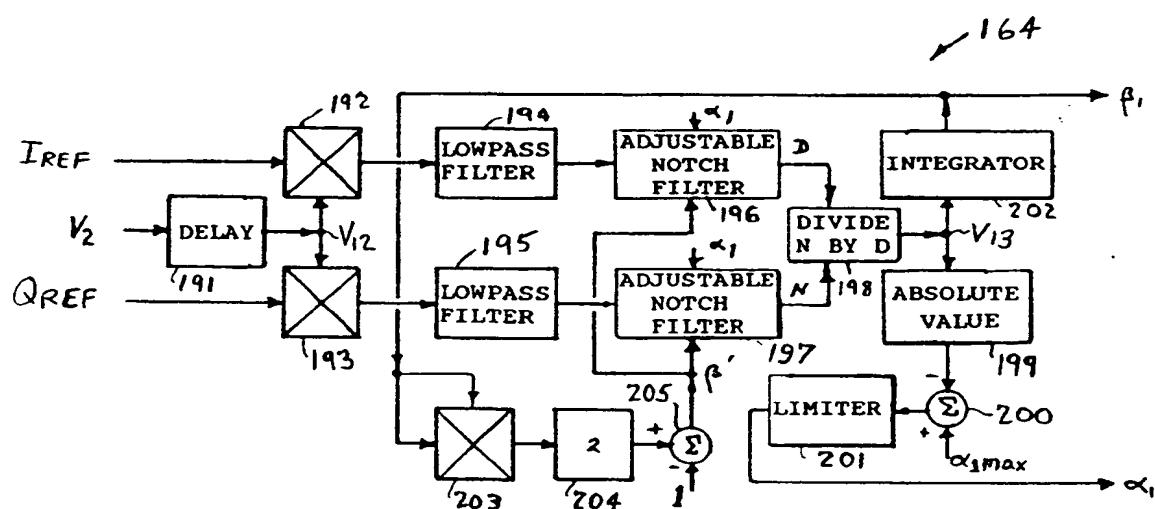
FIG. 18
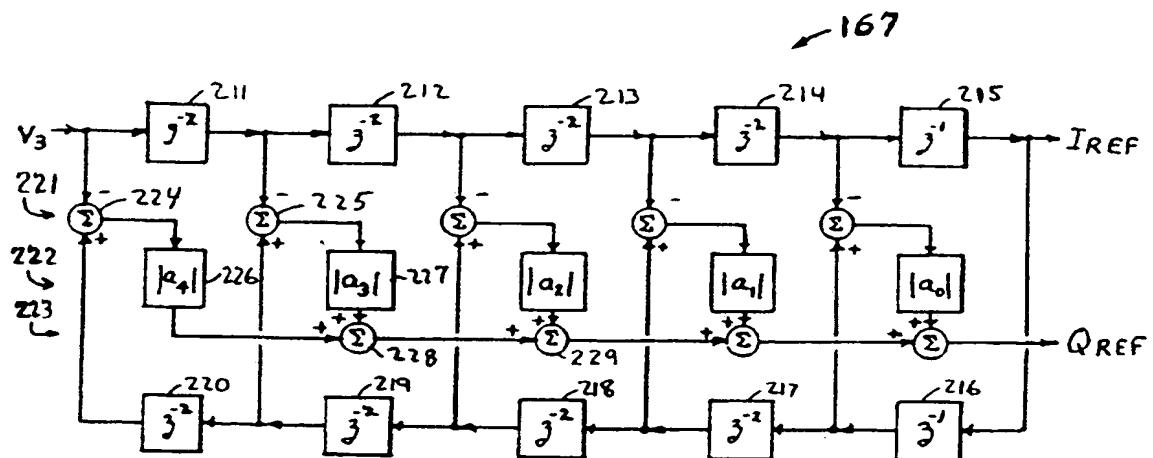
(PRIOR ART)   FIG. 19
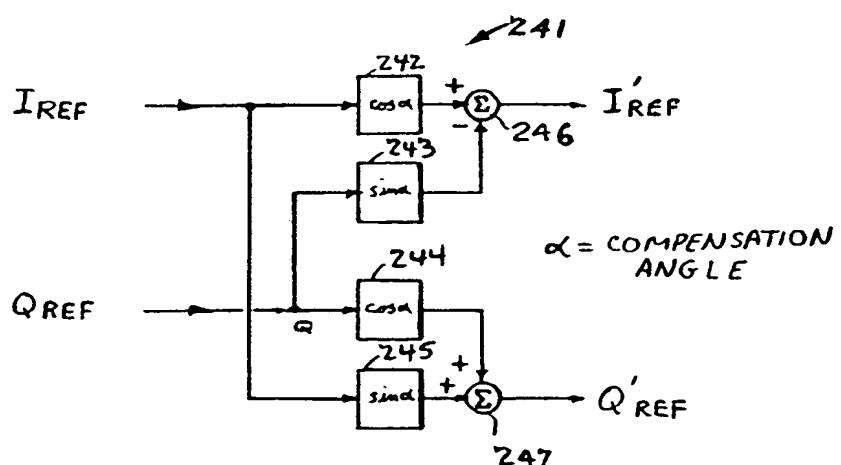
(PRIOR ART)   FIG. 20
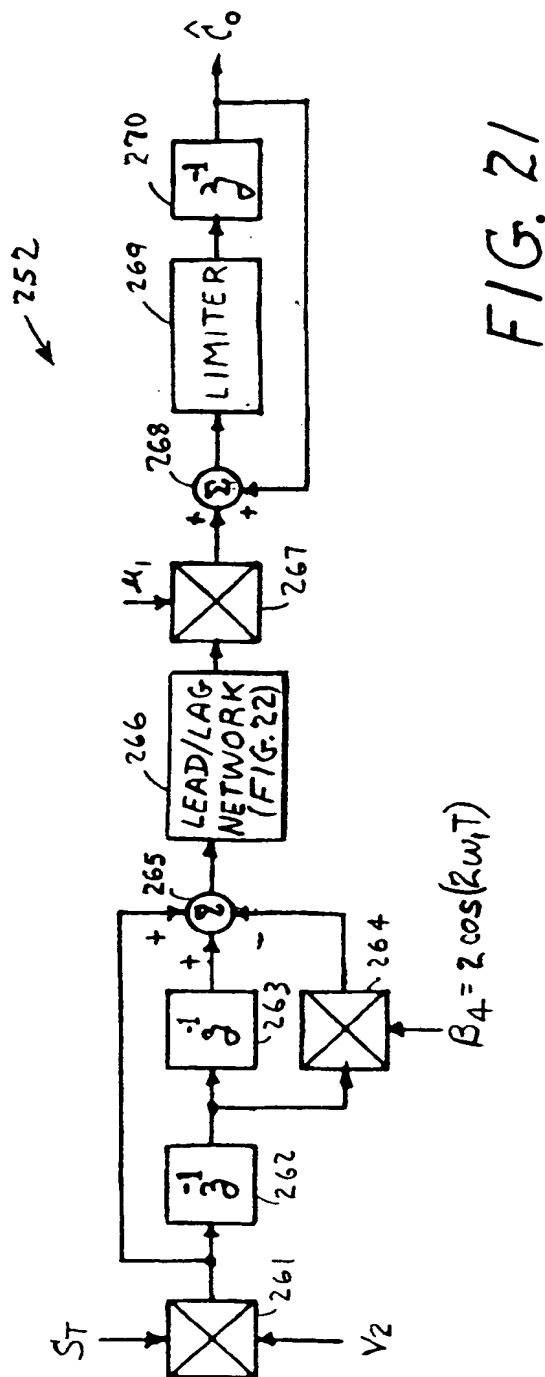
FIG. 21

FIG. 22
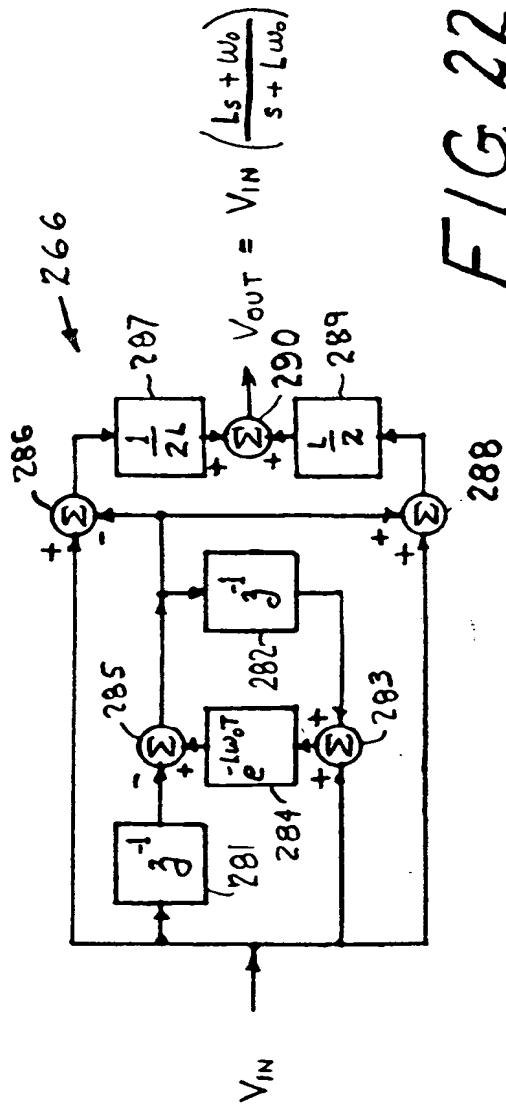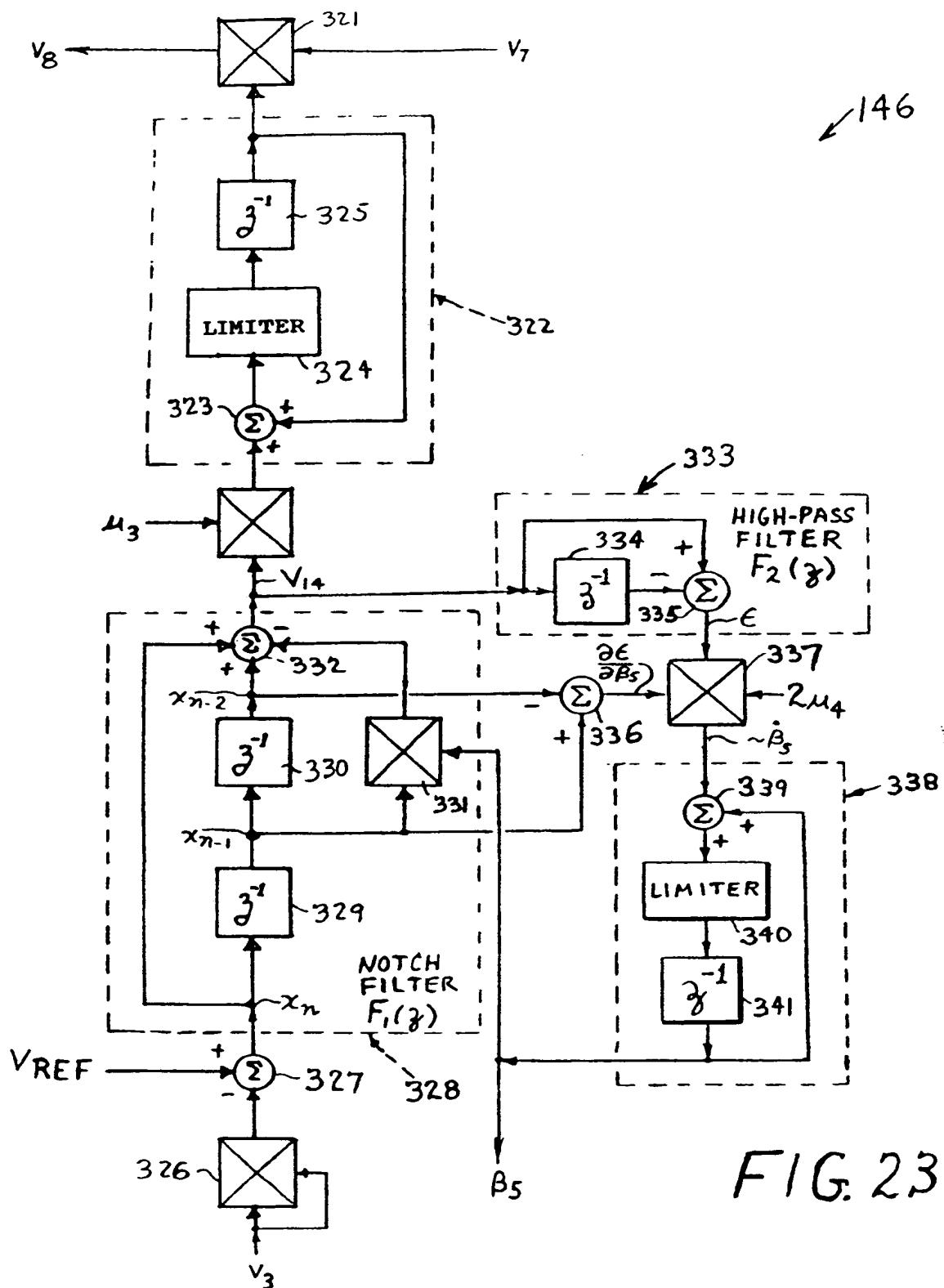
FIG. 23
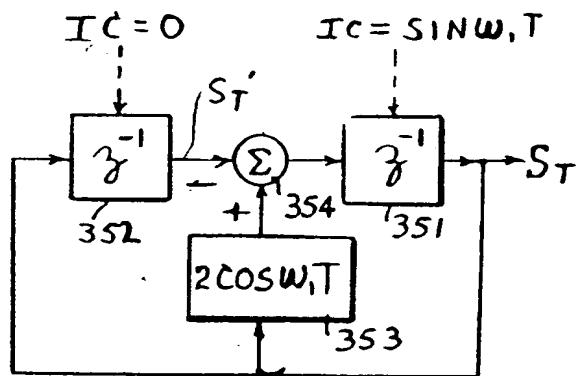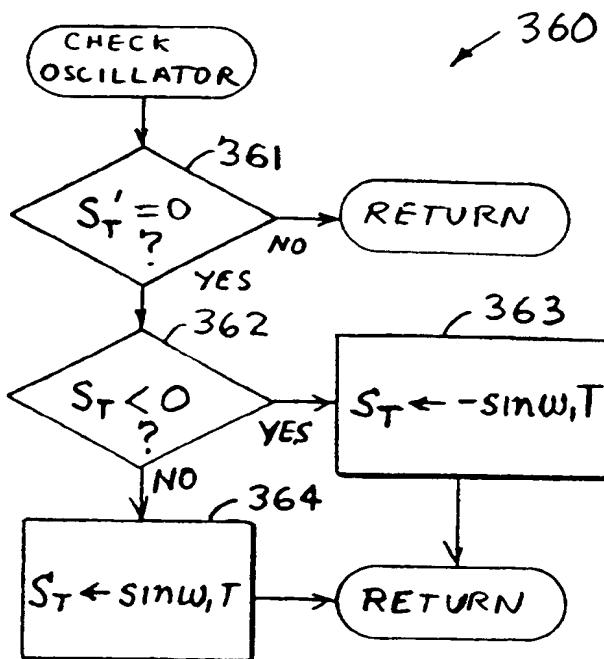
40

$$2\cos(2\omega_i T) \longrightarrow \beta_4 \qquad 253$$

FIG. 24

FIG. 25

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US-A-4 816 770 (NAUMANN) * figure 12 *	1,6	H03D3/00 G01C19/56
A	MACHINE DESIGN, vol.64, no.19, 24 September 1992, CLEVELAND US page 32 'Solid-state gyro borrows wristwatch technology'	1,6	
A	US-A-4 930 351 (MACY ET AL.) * figure 16 *	1,6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03D G01C H03J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 December 1994	PEETERS, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another
document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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